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Design and Optimization of 4-BIT Static RAM and 4-BIT Dynamic RAM for Compact and Portable Devices

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ABSTRACT

As technology advances, the combined compactness of transistors also increases. Portable electronics such as cellphones, notebooks, and laptops are in high demand. The enhanced innovation reduces the feature value for this compact design. Devices with a small feature set require less electricity to operate. The edge voltage is reduced when the power source is reduced. Low-limit devices perform better, but in such a deep submicron domain, sub-edge leakage current is critical. As a result, architects should focus on decreasing leakage. Several field workers have presented divergent ideas to explain this. A 4-bit static RAM cell using the reduction of the leakage power consumption (sleepy stack) technique and the 4-bit DRAM is proposed in this paper. The RAMs' schematic was produced using DSCH, and their layout was built using MICROWIND. Improved power consumption in static random-access memory by combining a sleepy stack with a keeper strategy and constructing a 4-bit dynamic random-access memory was explained as a result of this research. According to the findings, the higher the technology used, the higher the power consumption. On the other hand, after assessing the results, SRAM uses less electricity and has more transistors per memory.

1. INTRODUCTION

Today's devices rely heavily on semiconductor memory technology. Memory is utilized in any equipment that uses a CPU in one form or another and is often based on semiconductor technology [1]. The growth in popularity of CPUs has led to an increase in the use of semiconductor memory. While demand for semiconductor memory is on the rise, software in processors and computers is becoming more complex and large.

Initially, all processors and computers were made up of a CPU with only one hard disk, which has a speed of 80M-120MHZ, which is very slow to give data to the CPU in time. That is why RAM is placed between the CPU and the ROM, which operates at the same speed as the CPU. Later on, the CPU is updated with a multitasking processor; then it needs high-speed access memory that time RAM is divided into SRAM and DRAM.

Computers have shrunk in size, thickness, and weight with each generation. Smartphones and other mobile devices are no exception. It may fit in a pocket, be used as a portable game system, or be linked to a smartwatch or activity tracker. Although all of these devices are portable, not all of them are mobile. Although the phrase "portable device" has been in use longer than "mobile device," it has no agreed meaning.

A portable gadget is tiny and light to move around and carry with ease. The Osborn 1, the world's first laptop computer, weighed in at a whopping 24 pounds and was considered a portable computer. The phrase "portable" refers to anything that can be carried around, from a portable printer to a smartphone that can be put in the pocket. Before laptops and cellphones were widespread, the word was used far more frequently, maybe because there was a more precise separation between items that could be transported easily and those that could not. This project discusses the design and optimization of 4-bit SRAM and 4-bit DRAM for compact and portable devices.

This paper is set as follows: After the introduction, the details of the literature review are discussed in Section 2. Section 3 focuses on the research methodology, Section 4 is about the existing SRAM cell, and Section 5 is about the reduction of the leakage power consumption. Section 6 focuses

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on the existing DRAM cell. Section 7 elaborates on the proposed work, and Section 8 discusses the overall project. Finally, Section 9 is the conclusion of this project.

2. LITERATURE REVIEW

The literature for this study summarizes as in Table 1.

Table 1. Summary of literature review.

S.NO	Author(s) & Year	Title	Variables Studied/ Research Design	Important Findings
1	(Chandra Mishra and Singh, 2019) [2]	Design and Analysis of Low Power SRAM using CMOS Technology.	• For image/video processing applications, this study presents a novel SRAM system that decreases leakage power.	• This study outlines a novel column-based Energy Compression technique for reducing SRAM power consumption by selectively turning off cells based on data patterns. • Power savings in commercial CPUs and application-specific integrated circuit SRAM memory are detected using this technology. • The research also looks at how editing photos before storing them impacts power savings and data cluster topologies.
2	(Madhumalini and Saranraj, 2019) [3]	Design of Low Power Memory Architecture using 10t SRAM Array.	• The suggested 10T SRAM design discusses the problem of hold power dissipation. • There are ten transistors in the circuit, two of which are used as sleep transistors.	• The proposed memory architecture reduces power by 15% and delays by 45% compared to the current memory design.
3	(Lourts Deepak et al., 2018) [4]	28 nm FD-SOI SRAM Design Using Read Stable Bit Cell Architecture.	• The suggested bit cell is compared to a standard 6T bit cell in terms of access time, read stability, on-current, off-current, and sensing amplifiers and decoders.	• The recommended SRAM architecture delivers faster access time and reads stability than regular 6T SRAM. • A 28 nm FD-SOI platform was used to implement the design.
4	(A. S. V. S. V. P. D. Kumar et al., 2018) [5]	Stability and Performance Analysis of Low Power 6T SRAM Cell and Memristor Based SRAM Cell using 45NM CMOS Technology.	• This article is about developing low-power SRAM with 6T SRAM and memristors.	• By increasing the packing density to the point where the system is on-chip (SOC), the stored data limit can be reduced without using a power source, minimizing leakage current.
5	(Anudeep Varma and Sasipriya, 2020) [6]	Low power SRAM using Adiabatic Logic.	• Using 8T adiabatic SRAM and 2PADL SRAM, this work produced an SRAM memory cell.	• According to the results, the proposed 8T SRAM cell reduces power dissipation by roughly 25%, while the 2PADL SRAM cell reduces power usage by 70%.
6	(Shalini and Rajendar, 2017) [7]	CSI-SRAM: Design of CMOS Schmitt trigger inverter-based SRAM cell for low power applications.	• A low-voltage, radiation-hardened Static Random-Access Memory (SRAM) bit cell with exceptional soft-error robustness was presented.	• When compared to a 13T SRAM cell-based memory architecture, the recommended SRAM cell reduces delay by 65-70 percent, reduces power by 80-85 percent, and boosts read stability by 60-70 percent.

3. METHODOLOGY

The simulations are based on MICROWIND and DSCH tools. Designers can use the MICROWIND programme to model and design integrated circuits down to the physical description level. DSCH (Design Schematic Editor Tool) is an application that lets users edit schematic designs. DSCH is a logic editor as well as a simulator. DSCH is used to test the architecture of the logic circuit before beginning microelectronics design [8]. This project was started with the 4-bit SRAM. In DSCH, the work was saved first. Next, the foundry was set to 90 nm. Then, the circuit was designed correctly to avoid any errors during compilation. After the circuit was constructed, the "File" option is clicked, then "Make Verilog file" is selected to view the Verilog script. Then, the "Schema to new symbol" is chosen to view the symbol preview. In the "Schema to Symbol" window, the file is made sure to be saved in the specified directory. After that, in MICROWIND, the "Compile" option is clicked, and the "Compile Verilog File" is selected. The file is opened to perform the Verilog compilation into a layout, and the waveform for 90nm was obtained. By following the same processes, the results for 65nm technology of the 4-bit SRAM and DRAM were obtained. The components like n-channel MOS, buttons, connecting wires, inverters, and LEDs were used.

4. EXISTING SRAM CELL

4.1 Basics of SRAM

SRAM (static random-access memory) is a random-access memory that stores data in latches or flip-flops and keeps it for as long as power is delivered continuously. SRAM is a semiconductor memory that stores each bit using bistable latching circuitry. Data remanence is present in SRAM but lost when the memory is turned off [9]. Therefore, the stability and area of the SRAM must be considered when building an SRAM cell. The SRAM cell must write and read data and keep it for as long as the power is turned on. For nearly four decades, CMOS devices have been reduced in size to increase speed, performance, and power consumption. The single SRAM cell is shown in Figure 1.

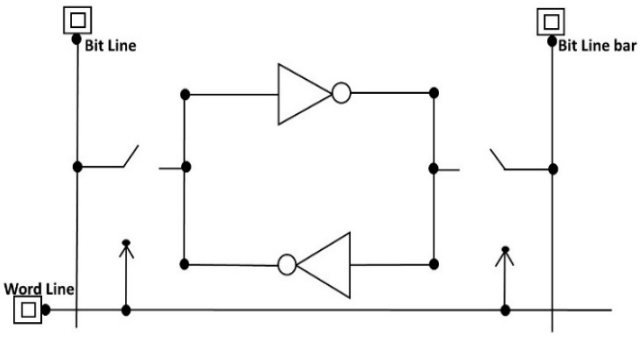

Fig. 1. The Single SRAM cell

4.2 SRAM Cell Design

Figure 2 depicts a single CMOS SRAM cell. Cross-coupled CMOS inverters are employed in the design of low-power CMOS inverters. In a cross-coupled inverter circuit, the static power dissipation is minimal. The circuit does, however, have a significant amount of leakage current. Two access transistors are coupled back to back in a single memory cell, and a simple CMOS inverter is present [10]. The two access transistors are turned on when the word line is active.

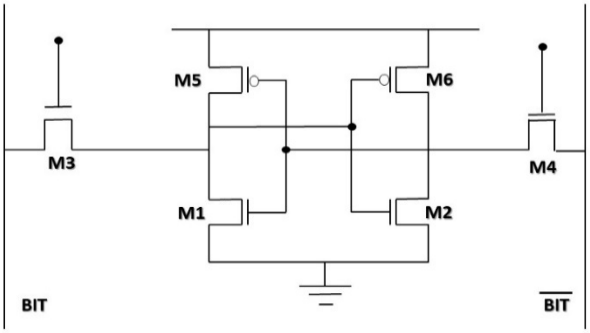

Fig. 2. SRAM Cell using CMOS

4.3 6T SRAM Cell

There are three states in an SRAM cell:

- Standby, which indicates that the circuit is not in use.
- Reading signifies that data has been read.
- Writing, implying that the details have been updated.

The two operational modes of SRAM are read and write, and read and write stability can analyse noise [11]. The states mentioned above work in the following way, as stated below. A 6T SRAM cell is depicted in Figure 3 is a block diagram.

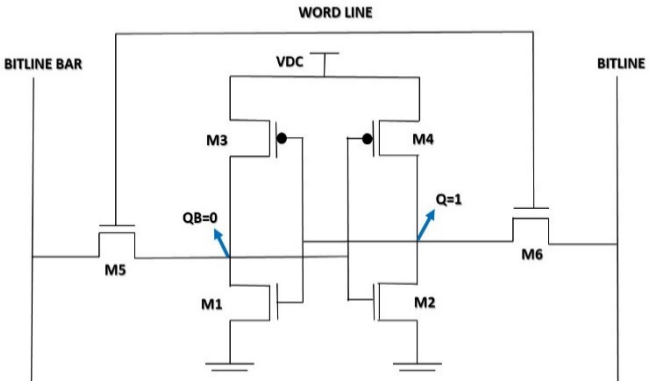

Fig. 3. 6T SRAM Cell Block Diagram

A. Stand By Mode

When the word line is not asserted, the access transistors M5 and M6 disconnect the cell's bit lines [12]. M1-M4 construct two cross-coupled inverters that enhance each other until the power source is connected as feedback.

B. Reading Mode

Assume that the memory's content is a 1 at Q. Sensing amplifiers collect data and produce output during the reading process. The row and column decoders read the data from the required cell or cells, and the information is then transmitted to the sense amplifiers via the transmission gate.

C. Writing Mode

A write cycle begins with the value to be written being applied to the bit lines. Set the BL bar to 1 and the BL bar to zero to write a zero. To produce a 1, the bit lines' values are inverted. After stating WL, the value to be saved is locked in.

The bit line input drivers may easily override the initial state of the cross-coupled inverters since they are significantly more potent than the cell's comparatively weak transistors.

5. The Reduction of the Leakage Power Consumption

In operation, the sleepy stack approach combines sleep transistor technology with a stacking strategy in idle mode. The actual transistor is split into two equal-sized transistors, and the sleep transistors s and s' are attached to each of the branched transistors in the same way as in the stacking technique, as shown in Figure 4. The two parallel transistors become active while the circuit is in standby (idle) mode, lowering the circuit's efficient resistance and resulting in a shorter propagation delay[10] [13]. The sleepy transistor is turned off when the circuit is turned off, and the stacked transistor lowers the leakage current.

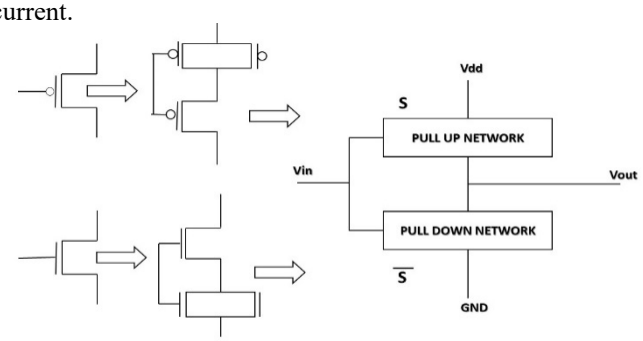

Fig. 4. The Reduction of the Leakage Power Consumption Approach

6. DRAM Cell

DRAM (dynamic random access memory) is a type of memory with a simple structure, smaller, and has a higher density than other memory types. The capacitor contains binary data. The presence or absence of the charge stored in the capacitor determines the value of the *stored* bit [14]. When the charge stored in the capacitor varies due to a leakage path between the source and substrate, called Dynamic, the information stored in the capacitor degrades. A 1T DRAM cell is shown in Figure 5

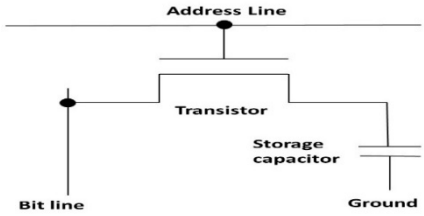

Fig. 5. 1T DRAM Cell

A. *Write Operation*

Both bitlines and uncharged capacitors can be charged using the writing function.

B. *Read Operation*

A bit line voltage is discharged to the ground during reading operation through the transistor; a high voltage charged the gate. Because the voltage stored at the node is preserved during the read operation, the read operation is non-destructive.

7. Proposed Work

7.1 *SRAM*

In the sleeping stack structure, there are two methods for reducing leakage. First, sleep transistors with high voltage transistors and transistors parallel with the sleep transistors reduce leakage power. Second, the stack effect, which is created by stacked and switched-off transistors, is another example. Figure 6 depicts the 4-bit SRAM's schematic diagram.

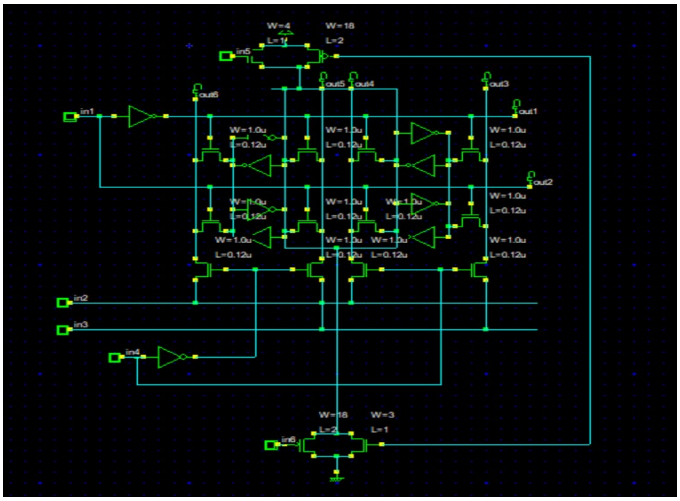

Fig. 6. The Schematic Diagram of the 4-bit SRAM using Sleepy-Stack and Keeper

Figure 7 shows the correspondence layout concept for 4-bit SRAM with a sleepy stack. Figures 8 and 9 depict the waveforms of the operations at different technologies.

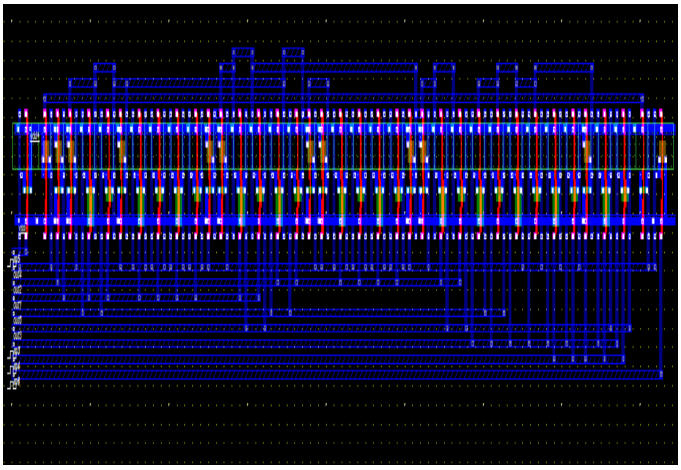

Fig. 7. Layout design of 4-bit SRAM with sleepy stack

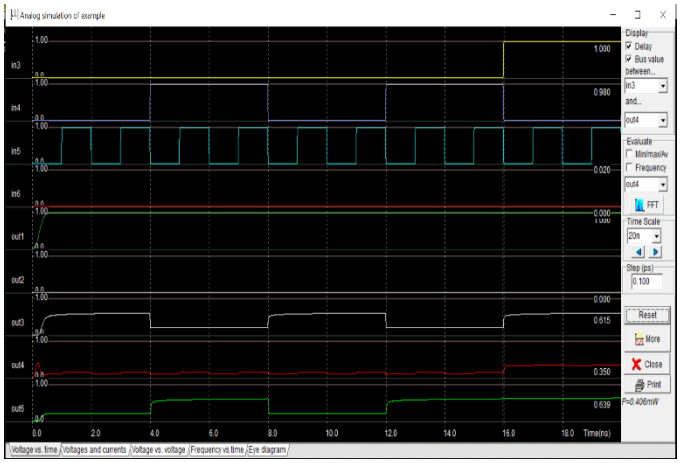

Fig. 8. Waveforms of 4-bit SRAM cell at 90nm technology

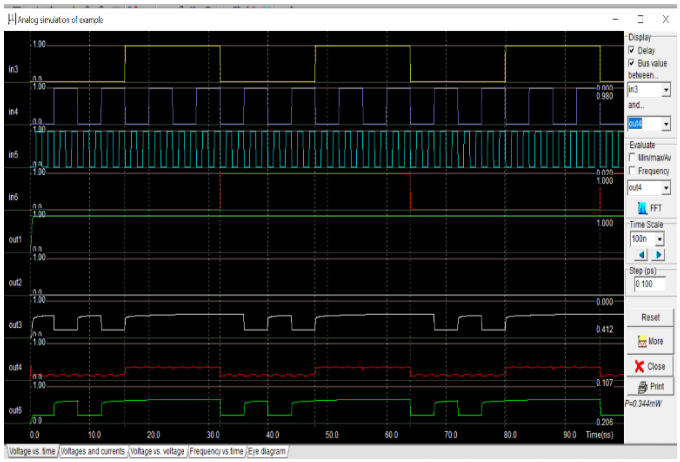

Fig. 9. Waveforms of 4-bit SRAM cell at 65nm technology

7.2 DRAM

The MICROWIND tool is used to implement the 4-bit DRAM cell correspondence structure. Figure 10 is represented below. Figures 11 and 12 depict the waveforms of the DRAM cell.

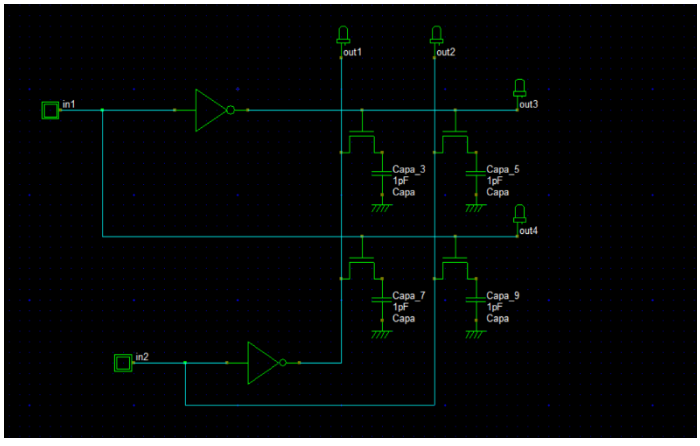

Fig. 10. 4-bit DRAM schematic

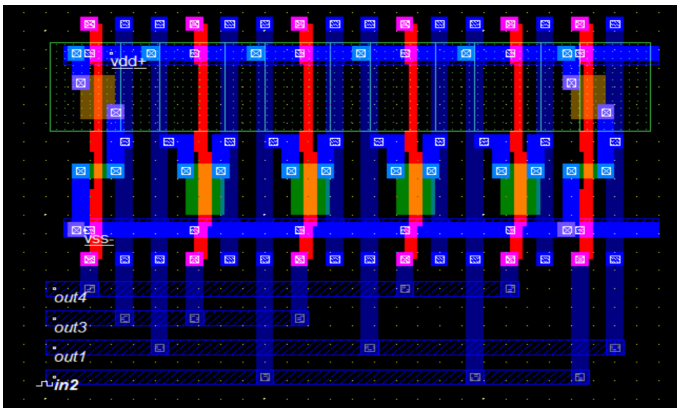

Fig. 11. Layout of 4-bit DRAM

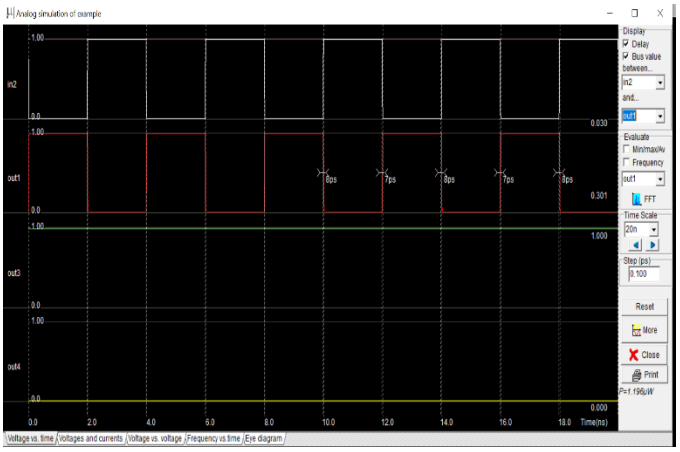

Fig. 12. Waveforms of DRAM at 90nm technology

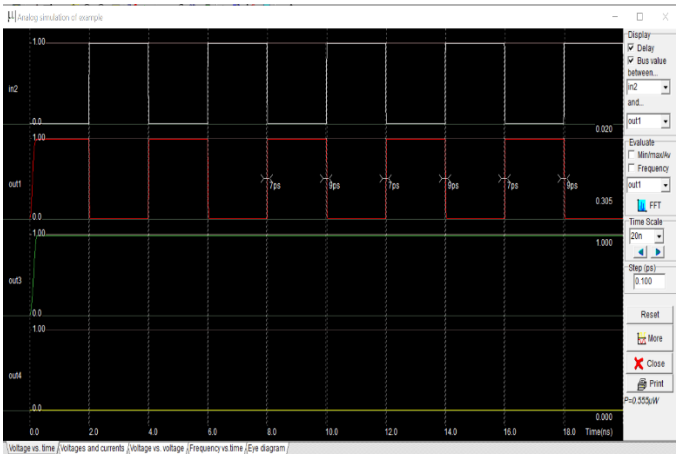

Fig. 13. Waveforms of DRAM at 65 nm technology

8. DISCUSSION

For this project, an investigation was carried out by varying the technologies. The project was started with the 4-bit SRAM using sleepy stack with the keeper and then continued with the 4-bit DRAM. Table 2 shows the results obtained for the research that has been conducted.

Table 2. The power consumption of different techniques.

Techniques	Technologies	Power Consumption
4-bit SRAM	90 nm	0.406mW
4-bit SRAM	65 nm	0.344mW
4-bit DRAM	90 nm	1.196µW
4-bit DRAM	65 nm	0.555µW

As a result, it can be noticed that the higher the technologies used, the higher the power consumption is. Besides, by analysing the results obtained, it can be seen that SRAM uses less electricity and more transistors per memory [15]. The DRAM consumes higher power than SRAM; however, DRAMs are one of the most extensively utilized varieties of RAM due to their simple, lightweight, and cost-effective construction [16].

The advantages of SRAM are it is easy to use. SRAM consumes less power than DRAM, which can be seen from the results. Since SRAM is highly reliable, it is commonly utilized as cache memory in computer systems. Besides, DRAM has some advantages over SRAM, including the fact that it is substantially less expensive. As a result, it is commonly utilized as the main memory. It has a large storage capacity as well as DRAM has a simpler structure than SRAM.

9. CONCLUSION

In conclusion, by carrying out this research, improving power consumption in static random-access memory by combining a sleepy stack with a keeper strategy and designing a 4-bit dynamic random-access memory were explained. For this project, DSCH was used to develop the schematics, while MICROWIND was used to implement the layout. The results obtained show that the higher the technologies used, the higher the power consumption is. On the other hand, by analysing the results obtained, the SRAM uses less electricity and more transistors per memory. Besides, DRAM consumes more power than SRAM, but it's simple, lightweight, and cost-effective design is one of the most widely used types of RAM. Hence, the proposed idea can be used in small, portable devices that operate over many frequency bands, such as cellular phones, tablets, and Wi-Fi routers.

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