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Design and Analysis of Full Adder Using 0.6 Micron CMOS Technology

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ABSTRACT

The design of a full adder involves the use of logic gates so that the design can convert 8 inputs to create a byte-wide adder and to force the carry bit to the other adder. However, the uses of multiplexers to replace the logic gates in the construction of the full adder is proven to be possible due to the function of the multiplexers to act as the digital switch in the system that provides the flow of digital information from multiple inputs into an output. This research aims to explore the possibility of implementing the multiplexers into the design of the full adder and to analyse the different possible full adder design using the multiplexers. Using the multiplexers also allows for fewer logic gates to be used in the design of the full adder, which reduces the overall area coverage of the full adder. However, adding multiplexers does not make a complete adder more efficient and may slow it down. Thus, this article compares a conventional full adder with logic gates, a full adder with two 2:1 multiplexers, and a full adder with six 2:1 multiplexers in terms of power usage, time delay of the Sum and Carry outputs, and technology (0.6 μm).

1. INTRODUCTION

In a digital logic, a full adder is a adder which consists of three and two outputs. Z.Zain recognized the full adder being one of the most important digital blocks for a lot of systems [1]. This is mainly due to the ability of the full adder to perform mathematical operations such as addition or subtraction for the digital circuits. A basic full adder design combines two binary digits (A, B) alongside a carry-in digits (Cin) inputs and creates a sum (Sum) and a carry-out (Carry or Cout) output.

Fig. 1 *The design of a One-bit full adder cell [2]*

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Table 1 *Truth table of a One-bit full adder cell.*

Button State			Output	
A	**B**	**Cin**	**Carry**	**Sum**
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

The truth table of a full adder is shown in Table 1. Through the truth table, the Sum output can be summarized into a Boolean expression:

$$\text{Sum} = A \oplus B \oplus \text{Cin} \quad (1)$$

The carry-out (Cout or Carry) output meanwhile is summarized into the Boolean expression as below

$$\text{Carry} = A.B + B.\text{Cin} + A.\text{Cin} \quad (2)$$

[2] further explains the functionality of the full adder, in which that any number of full adders can be linked together through the Carry-in input and Carry-out outputs to form an *n*-bit addition, as illustrated on Fig. 2:

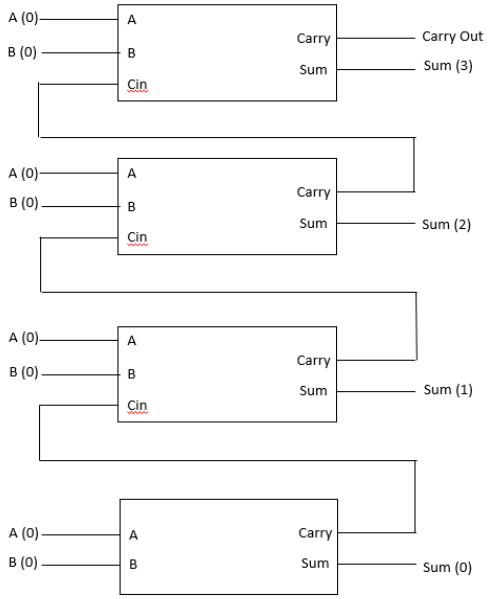

Fig. 2 *4 Full adders being connected into a 4-bit adder.*

In a conventional full adder design, the circuit mainly consists of two XOR gates, two AND gate and one OR gate. The design of the conventional full adder is shown in Fig. 3 below:

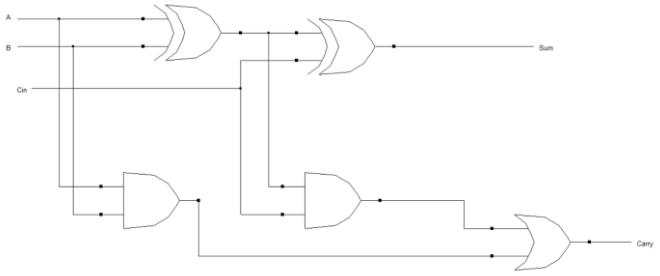

Fig. 3 *shows the conventional full adder [3]*

In a typical full adder, Sum is obtained through the XOR function of the inputs, while the Carry is the same as the previous logic gate when two of the inputs have the same state [3]. A multiplexer (MUX), sometimes is being called as a data selector, is a component that choose several analog or digital inputs and filter them into one output. [4] further explains that the multiplexer is capable of altering parallel data into serial data by redirecting such data from many inputs into one output. The multiplexer comes in variety, with the different number of inputs define each variation, such as 2 to 1 MUX, 4 to 1 MUX, 8 to 1 MUX and 16 to 1 MUX. A multiplexer can be built using the logic gates, in which the 4 to 1 Multiplexer is shown in the Fig. 4, with the Truth table of that multiplexer shown in Table 2.

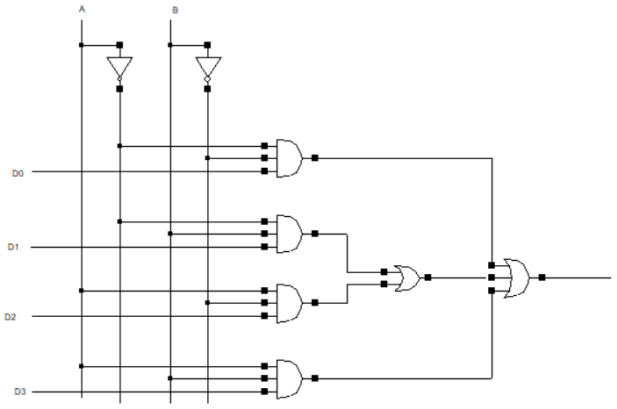

Fig. 4. *4 to 1 Multiplexer built using Logic gates [4]*

Table 2 *Truth table of a 4 to 1 Multiplexer [4]*

Inputs		Output
A	**B**	**Y**
0	0	0
0	1	1
1	0	0
1	1	1

[4] also proposed that using multiplexers in a combinational circuit can allow for a more cost-efficient and less complications, this includes the use of multiplexers in a full adder. However, as more multiplexers is used, the delay of the full adder will increase as well due to the port-switching and extra I/O (Input/Output) signals that increases as more multiplexers is added. Previous works have been covered in [12] and [13] respectively.

2. LITERATURE REVIEW

The variety of the design on a full adder is retrieved and compared from the other writers or authors that experiments with the same topics. [5] had designed a low power full adder high speed full adder that have better performance than the conventional full adder. [6] demonstrated their quaternary full adder designs which also provides positive results from the performance of their full adder design.[7] has their design on the full adder to be more area efficient and low powered which uses Multiplexers into the design. [8] showcases their take on the full adder design that uses six multiplexer gates, which will be then replaced with two transistor Multiplexers that gives the MBA-T12 cell. Finally, [9] also proposed another full adder design that also uses six Multiplexers gates with all of the internal gate nodes directly inputed with fresh signal for faster transitions to output signals. The details on the design of the full adders from the authors are mentioned further in table 3.

Table 3 *Literature Review of Full Adder using CMOS Technology*

No	References	Title	Research Design	Important Finding
1	[5]	Design & Study of a Low Power High Speed Full Adder Using GDI Multiplexer	Using six 2T multiplexers through the GDI (Gate Diffusion Input), the authors design a low power full adder circuit. The GDI technique provides with different types of logic function using two transistor-based circuit arrangement. A basic GDI will consist of 3 inputs and is made up of one nMOS and one pMOS.	The proposed full adder from the authors have seen to have improvement in term of the full adder delay, power and area coverage when compared with the conventional full adder.
2	[6]	A Novel Multiplexer-Based Quaternary Full Adder in Nanoelectronics	The proposed full adder design uses quaternary positive 2:1 multiplexer, quaternary 4:1 multiplexer, quaternary successor, predecessor and second level successor. In the full adder design, the quaternary inverter is utilized as well.	The proposed full adder in the three-supply voltage case has low level of PDP, with the result being 1590 times lower than the greatest recorded result. In a single supply voltage case, the PDP is also reduced to about 3.04 of that of the best reported single supply voltage design.
3	[7]	Design of Area Efficient and Low Power Multipliers using Multiplexer based Full Adder	In the design of the full adder, the author uses the multiplexer based full adder into the multiplier circuit which included the modified wallance and truncated multiplexers. The Wallance multiplier consists of partial product by N^2 AND gates, while the Truncated multiplier uses constant correction method or variable correction procedure.	The modified truncated multiplier improves much more in device utility through the reduction of the area coverage when compared to modified Wallance multiplier, which offers up to 25% less area coverage as well as 10% less power and hence is considered an efficient in power dissipation reduction and maintaining less area coverage.
4	[8]	A Novel Low Power Multiplexer-Based Full Adder Cell	The Authors introduce a 1-bit full adder design that uses six multiplexer gates. The multiplexer gates is replaced with 2-transistor Multiplexer that gives the MBA-T12 cell that in total use 12 transistor to realize the 1-bit full adder design.	When comparing the proposed design to the conventional design, the modified version is shown to save more than 26% power when testing under 6 different frequencies and loads using H-Spice.
5	[9]	A Novel Low Power Multiplexer-Based Full Adder	The proposed full adder design uses six identical Multiplexer gates which will be then replace with 2 transistor circuit. All of the internal gate nodes are directly inputted with fresh signals to create a faster transition into the output signals.	Compared to the most power efficient 10-transistor adders, the proposed design uses 23% less power and is 64% more faster than the recorded fastest tested adders.

3. RESEARCH METHODOLOGY

Most of the research have discovered that when using multiplexers in a full adder, the full adder improved in the power usage, the speed of operation as well as the efficiency of the full adder. However, none of the research done suggest the optimum design on the full adder when their research is completed and provide the conclusion based on one design. Hence for research methodology in determine the optimum design of a full adder, three full adder design will be simulated using the DSCH Software which is followed up in the Microwind Software for simulation.

3.1 Conventional Full Adder

The design of the conventional full adder follows the default full adder design, in which it uses Logic gates in the construction of the full adder. Using 2 XOR gate, two AND gate and one OR gate, the conventional full adder is built which contains three inputs (A, B, Cin) and two output (Sum, Carry). The design of the conventional full adder will follow Fig. 3 as a point of reference.

3.2 *Modified Full Adder version 1 (Using two 2:1 multiplexers).*

Using the proposed model from Maurya et al., the Modified Full Adder version 1 will be constructed using two multiplexers. Alongside the design, an XOR gate as well as a NOT gate is used in this modified full adder. This work, according to Maurya et al., display the study on the Wallance tree multiplier and the truncated multipliers in both this version of the full adder and the conventional full adder, which suggests that the modified full adder occupies less area when compared to the conventional full adder. Fig. 5 shows the design of the modified full adder version 1 that uses 2 multiplexers [10].

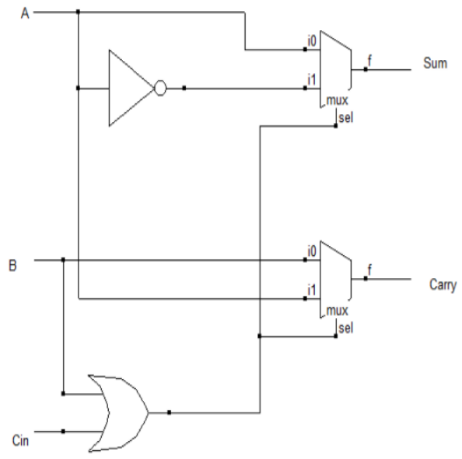

Fig. 5 *Modified Full Adder version 1 design.*

3.3 Modified Full Adder version 2 (Using six 2:1 multiplexers).

The proposed model for the Modified Full Adder version 2 using six multiplexers originated from the design of Fig. 6, where they use two 4 to 1 multiplexers. For the simulation, the design using two 4 to 1 Multiplexers is converted to six 2 to 1 Multiplexers. The conversion from 4 to 1 multiplexer to 2 to 1 Multiplexers increases the area coverage of the overall circuit due to the number of 2 to 1 multiplexer being triple the number of the 2 to 1 multiplexers on the Modified Full Adder version 1.

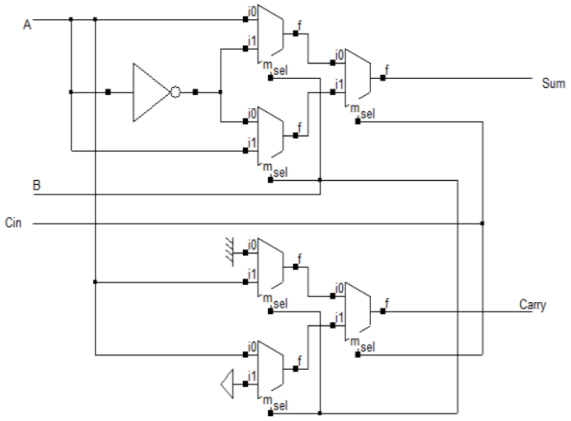

Fig. 6 D*esign of the Modified Full Adder version 2.*

4. RESULT AND DISCUSSIONS

The Schematics of the previously mentioned full adder Designs were created in the DSCH Software and is then compiled into the Microwind to check for the Power Usage and the Output Delay for three full adder Design. The simulation results are displayed from Fig. 7 until Fig. 15. Throughout the simulation, the 0.6 Micron CMOS Technology is used to ensure that all three full adder design are being tested in a similar environment and that the comparison between the three designs can be made fair. Additionally, 0.6 micron CMOS technology is used for the purpose of electronics development which will acts as a signal conditioning circuit in the three full adder designs, according to [11].

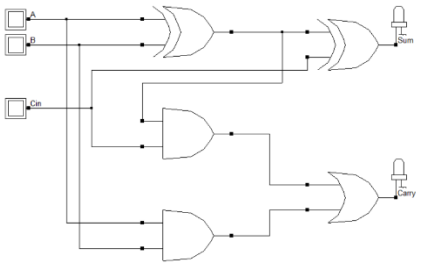

Fig. 7. *Schematic Circuit of the Conventional Full Adder in DSCH.*

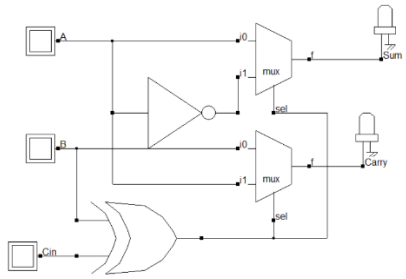

Fig. 8. *Schematic Circuit of the Modified Full Adder version 1 using two Multiplexer in DSCH.*

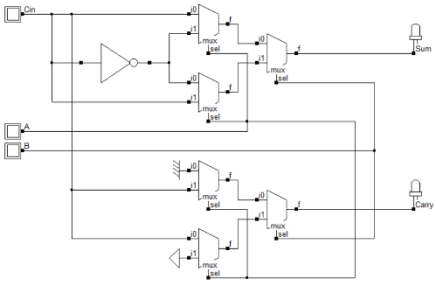

Fig. 9. *Schematic Circuit of the Modified Full Adder version 2 using Six Multiplexer in DSCH.*

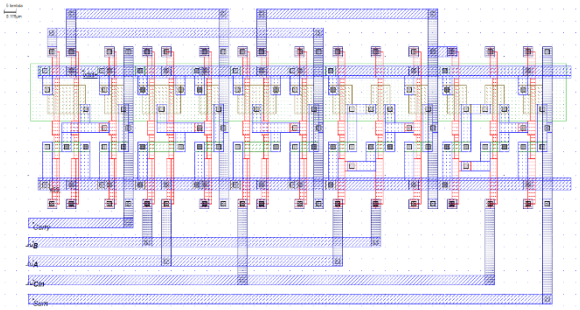

Fig. 10. *Layout Circuit of the Conventional Full Adder in Microwind.*

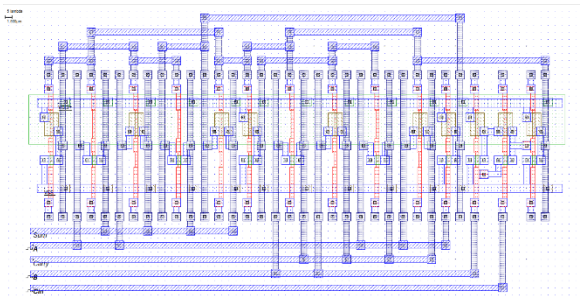

Fig. 11. *Layout Circuit of the Modified Full Adder version 1 using two multiplexers in Microwind..*

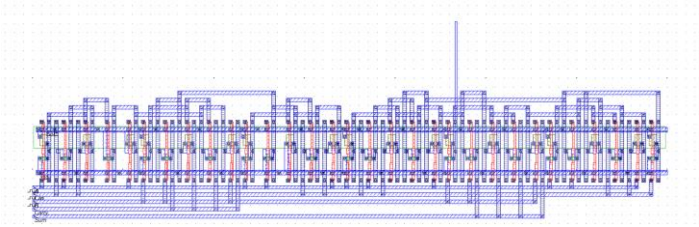

Fig. 12. *Layout Circuit of the Modified Full Adder version 2 using six multiplexers n Microwind.*

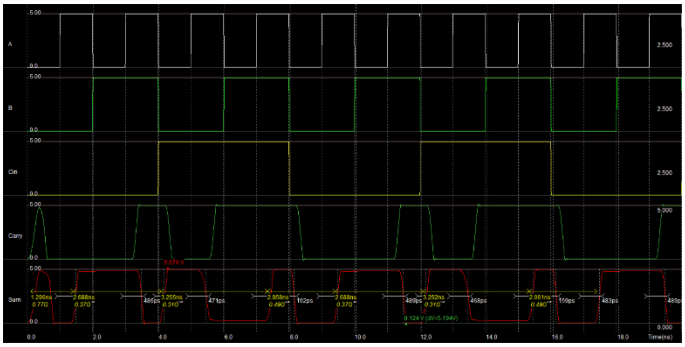

Fig. 13. *Pulse Operation for the Conventional Full Adder.*

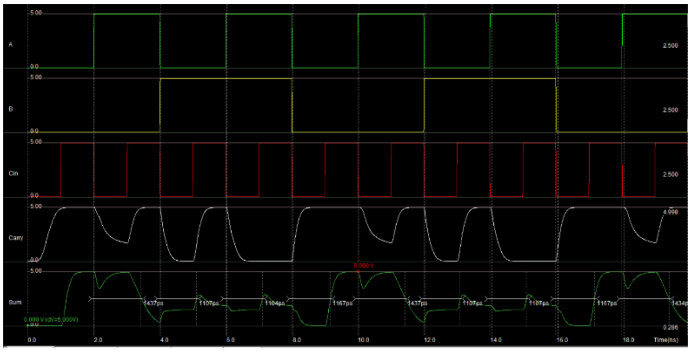

Fig. 14. *Pulse Operation for the Modified Full Adder version 1*

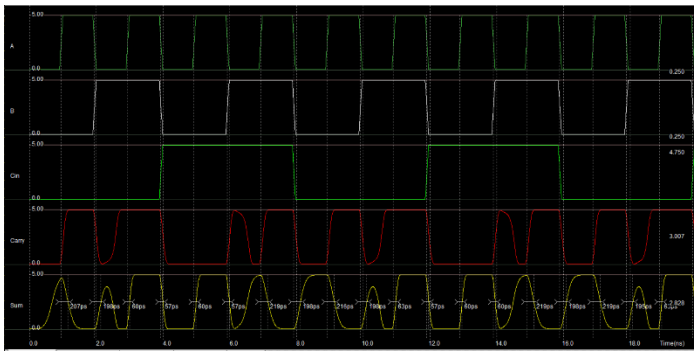

Fig. 15. *Pulse Operation for the Modified Full Adder version 2*

In each of the Pulse Operation diagram from Fig. 13 to Fig 15, the parameters of the I/O can be retrieved such as frequency, speed etc. However, for the experiment, the value of the minimum time delay for both outputs (Sum and Carry) as well as the power usage is collected and tabulated into a table format which is shown at Table 4.

Table 4 *Power Usage and Minimum Output Time Delay of each Full Adder Circuit*

FULL ADDER VERSION	MIN TIME DELAY IN CARRY (PS)	MIN TIME DELAY IN SUM (PS)	POWER USAGE (MW)
Conventional Full Adder	159	162	2.393
Modified Full Adder Version 1 (Using 2 Multiplexer)	63	57	2.144
Modified Full Adder Version 2 (Using 2 Multiplexer)	117	1104	3.442

Through the result gained from the simulation, the minimum time delay in the Version 1 of the full adder design is proven to be the shortest for both the Carry output as well as the Sum output. When compared to the conventional design, the time delay for the version 1 design for the Carry output is 60.38% less while for the Sum output is 64.81% less. In terms of power usage, the Version 1 design of the full adder is also shown to be the shortest as well, with 10% less power being used when compared with the conventional design. The minimum time delay of the Carry output in the Version 2 design is also shorter when compared to the conventional design, with around 26.41% less time delay. However, when checking the minimum time delay at the Sum output, the value is 10 times the time delay of that from the conventional design. The power usage for the Version 2 is higher than the conventional full adder as well, with 43.84% more power being used.

5. CONCLUSION

From the results, it is evident that the full adder that uses two multiplexers is among the most optimal setup for a high efficiency full adder construction since it uses less power but generate result with less delay when compared to the other two design. The full adder also occupies less area since it uses less components as well which contributes to it using less power as well. Hence, when implementing full adder for any system, it is recommended to use the modified full adder design that uses the two multiplexers to improve the performance of the systems, while producing the same logic as the other two design which is based on the truth-table produced on the result.

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