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Comparative Analysis of CMOS based Full Adders by Simulation in DSCH and Microwind

Sehan Amandu Gamage[1], Krishnan Subramaniam[1], and Ahmad Anwar Zainuddin[*2]

[1]*School of Engineering and Computing, Manipal International University, Negeri Sembilan, Malaysia.*
[2]*Kulliyyah of Information and Communication Technology, International Islamic University Malaysia*

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ABSTRACT

The decrease of surface area is a critical concern for any type of digital circuit. For example, the VLSI approach is used to lower the chip's size, which increases both the device's density and its performance. When it comes to digital circuits, a full adder circuit is a crucial part of any arithmetic processor. A computer, or any other type of computer, will have this component. Most arithmetic operations performed as of now are 64 bits. As a result, we need a sizable amount of room to complete this procedure. We can also take use of these advantages even if we increase the number of bits that need to be processed in parallel. This research attempts to demonstrate how a 4-bit CMOS-based full adder circuit is designed and simulated using Microwind and DSCH at various technology levels. It is then compared to determine if the transistor size may help achieve those benefits. Afterwards. A four-bit binary addition is the goal of the circuit that was built. A 4-bit full adder may be built using a totally automated CMOS design process. The concept and layout of a 4-bit full adder are developed in the initial CMOS design. With nodes of 90, 65 and 45 nm, the designs are produced and modelled utilizing technology. Digital integrated circuits with smaller nodes perform better when compared to those with larger ones, according to simulation findings and distinct outputs.

1. INTRODUCTION

One of the fundamental components of a digital computer as well as any form of microprocessor circuit that may be utilized in computers and mobile devices is referred to as a binary adder circuit. Adders are often found in the ALU, as well as other parts of computers and processors, for a variety of purposes, including calculating addresses and other tasks related to them. If adders are utilised elsewhere on the CPU, this is still true. These may be built in a variety of forms, including binary coded decimal and excess 3. Half adders and full adders are the two primary subcategories that make up the adder category. This study aims to demonstrate, using Microwind and DSCH, how a 4-bit CMOS-based complete adder circuit may be constructed and simulated at a variety of different technology levels. The results of this comparison are then used to establish whether or not the size of the transistor can contribute to the achievement of those benefits. Afterwards. The purpose of the circuit that was developed is to do a binary addition using all four bits. An entirely automated CMOS design approach might be used to create a whole adder with four bits of data. During the development of the first CMOS design, both the concept and the layout of a 4-bit complete adder were created. The designs are developed and modelled with the assistance of technology, using nodes of 90, 65, and 45 nm respectively. According to the results of simulations and individual outputs, digital integrated circuits with smaller nodes perform better than those with larger ones. This conclusion was reached after comparing the two types of circuits.

*Corresponding author:
E-mail address: Ahmad Anwar Zainuddin < anwarzain@iium.edu.my >.

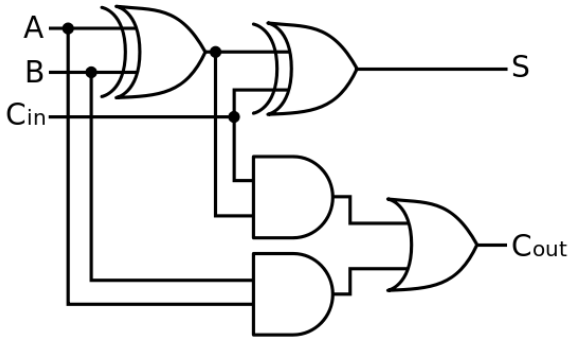


Fig 1. CMOS full adder

In very large-scale integration (VLSI), adders with varying bit widths are frequently required for implementation in everything from computers to specific embedded devices. In order to save even more power than supplemental TTL, logic type similarities that rely on entire CMOS chips have recently come to light.

Table 1. CMOS Full Adder truth table

Inputs			Outputs	
A	**B**	**Cin**	**Sum**	**Cout**
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1

Figure 1 shows a simple CMOS Full Adder, the most rudimentary form of a 4-bit CMOS full adder, A 4-bit full adder is essentially four 1-bit full adders placed in succession with each block receiving the carry bit of the previous adder as an input.

The structure of the paper is as follows: After this introductory material, Section 2 presents the literature review. Section 3 then discusses the design of project. Results analysis and discussion constitute Section 4. Finally, the paper's succinct summary is presented in Section 5.

2. LITERATURE REVIEW

The performance of a 1-bit full-adder cell is given in the work of Shams M. Modules of the adder cell are broken down into smaller parts. In-depth research and evaluation go into the modules. Each of these concepts has been designed, prototyped, simulated, and examined several times before finalising any one of them. To create twenty separate 1-bit full-adder cells (most of which are innovative circuits), these modules are connected in various ways. The power consumption, speed, size, and driving capabilities of each of these cells vary widely. Adder cells are employed in a simulation of two actual circuits. Circuit designers can choose from a variety of full-adder cells in a library that has been created for them, allowing them to focus on the tasks at hand. Figure 2 shows the adder design implemented in this study.

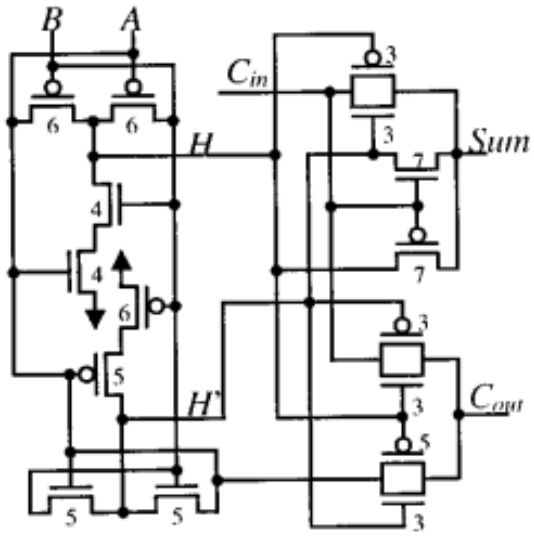


Fig. 2. Adder design implemented in study

In their paper, Sharma et al. [5] [4] describes an area and power efficient 56T 4-bit comparator architecture demonstrated by utilizing GDI [4]. 28 NMOS and 28 PMOS transistors make up the four-bit comparator architecture that has been presented. Full adder modules have been employed to develop this comparator, which uses less space and power at 120 nm than prior full adder modules. The suggested 4-bit comparator architecture is based on a 10T full adder module. Figure 3 shows the DSCH diagram of 4-bit full adder.

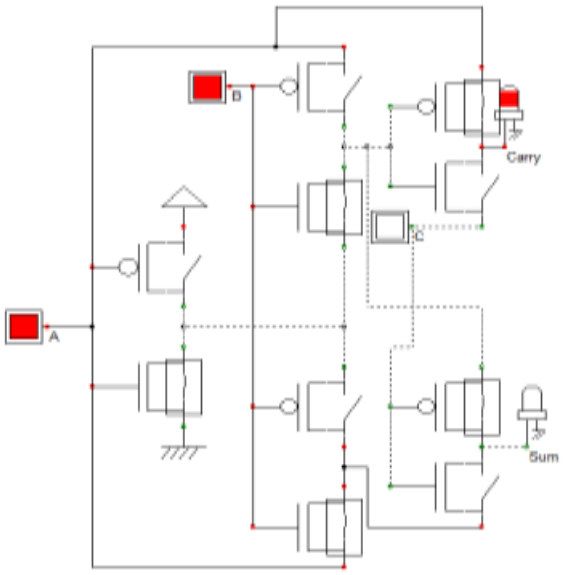


Fig 3. DSCH diagram of 4-bit full adder

An investigation of the effectiveness of a complete adder cell with a single bit was carried out, and the results are presented by Ahmed et al. in his paper. In this step, the adder cell is disassembled into its component pieces. Analysis and

feedback on the modules are performed often. Multiple designs for each are created, prototyped, simulated, and evaluated. Connecting various configurations of these modules results in twenty distinct 1-bit full-adder cells, most of which are unique circuits. [3]

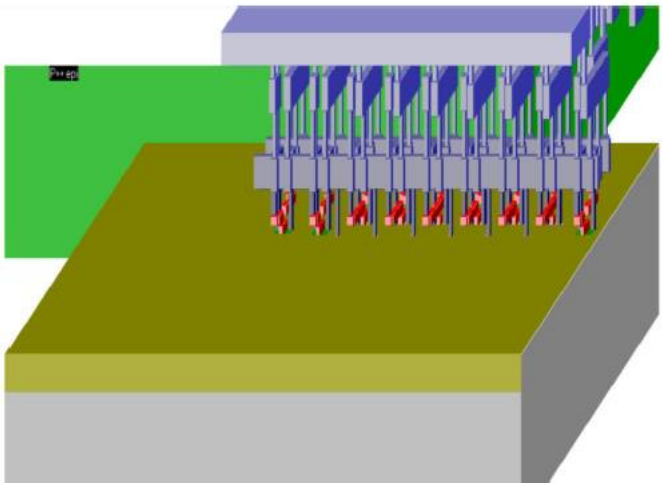


Fig. 4. 3-D interpretation of CMOS Full Adder

Singh et al. came up with a CMOS-based multi-threshold version of a 4-bit full adder to use in their research. During the standby state, the forward body biassed multimode (MTCMOS) technique is used to carry out the required measurements in order to estimate the leakage current, power consumption, and ground bounce noise. The 45 nm technology cadence virtuoso was used to conduct all of the simulations pertaining to voltage and temperature that are included in this paper [2]. Figure 5 shows the Multi threshold 4-bit full adder.

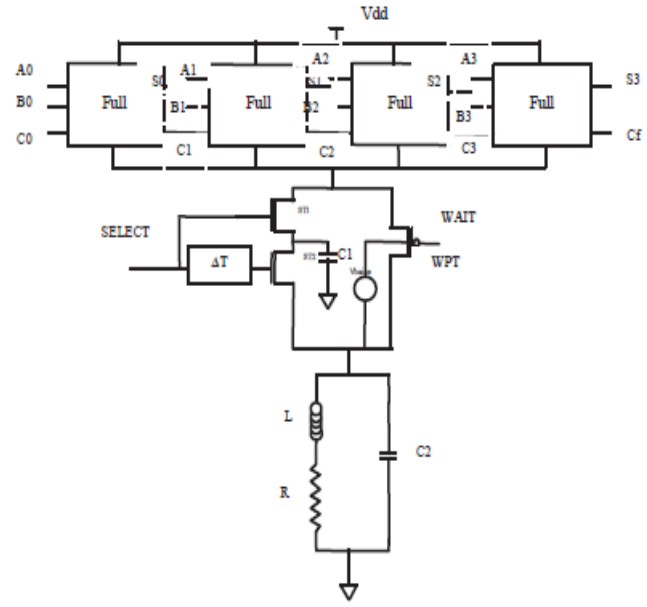


Fig 5. Multi threshold 4-bit full adder

The purpose of Albadry et al's study is to offer a design for a 4-bit multiplier that makes use of full adder cells and is founded on the full swing gate diffusion input approach[8]. The suggested adder design utilises a total of 18 transistors, and it is evaluated and contrasted with several logic styles for complete adders simulated with the use of cadence virtuoso, which is based on TSMC 65nm models and operates at a frequency of 250MHz with a supply voltage of 1v. Full adder design, according to simulation findings, uses the least power, occupies the shortest area, and provides full swing output voltage among the designs that were tested.The suggested complete adder was utilised to construct Array, Barun, and Baugh Wooley multipliers. In comparison to CMOS, the energy efficiency and the number of transistors in these multipliers were significantly increased.

3. DESIGN

The flow chart for the design implementation for this study is shown in Figure 6.

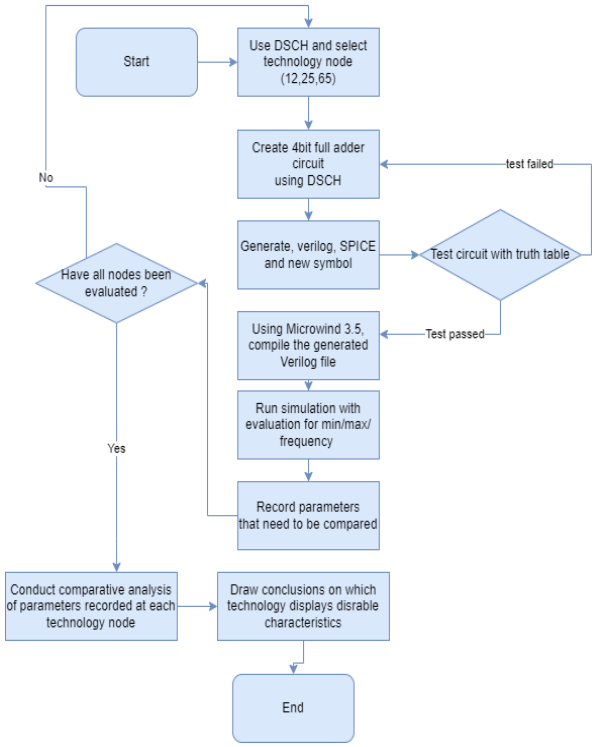


Fig 6. Flow chart showing design of study

4. RESULTS AND ANALYSIS

There are 56 nmos and pmos transistors have been in total have been used in this design providing for a balanced CMOS design. Figure 7 shows the transistor level diagram of the 4bit full adder once the Verilog file has been compiled in Microwind. Two voltages, 1.8V and 0.4V was input to simulate the binary value 1 and 0 respectively. Figure 8, Figure 9 and Figure 10 shows the simulation graph for 12 nm, 25 nm and 65 nm respectively.

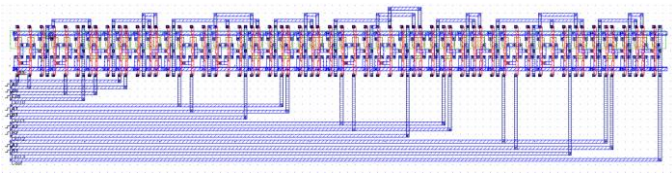


Fig 7. Transistor level diagram of 4-bit CMOS full adder

Fig 8. Simulation graph of 12nm

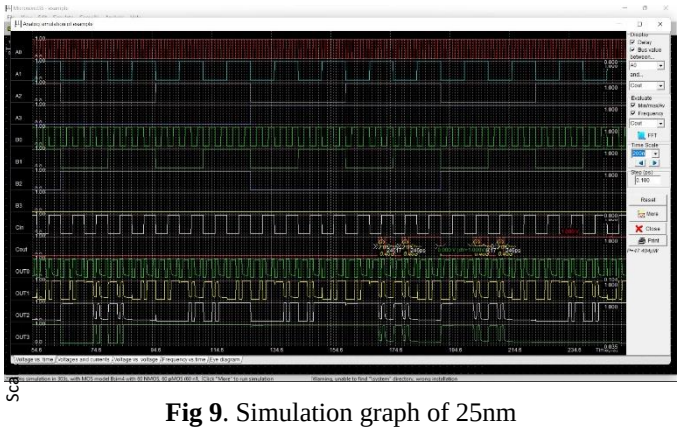


Fig 9. Simulation graph of 25nm

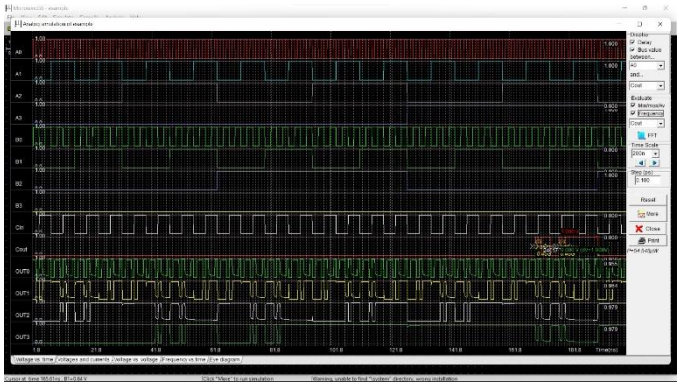


Fig 10. Simulation graph of 65nm

Area calculation and comparison:

To find the area required by each 4-bit adder, the area taken up by a 1-bit full adder is found.

Layout width = 16×8λ = 128λ nm
Layout length = 10×8λ = 80 λ nm
Area = 1024 λ 2 nm2
Area for 4-bit full adder = 1024 λ 2 nm2 x 4 = 40960λ2 nm2
Where λ = feature size/2.
Therefore, area required at each technology node:

- 12nm: $40960(12/2)^2$ nm2 = 1.475 μm^2
- 25nm: $40960(25/2)^2$ nm2 = 6.400 μm^2
- 65nm: $40960(65/2)^2$ nm2 = 43.264 μm^2

Table 2, table 3 and table 4 shows the area, average and power consumed at each technology nodes. m

Table 2. Area Required at each technology node

Technology Node	Area Required
12	1.475 µm2
25	6.400 µm2
65	43.264 µm2

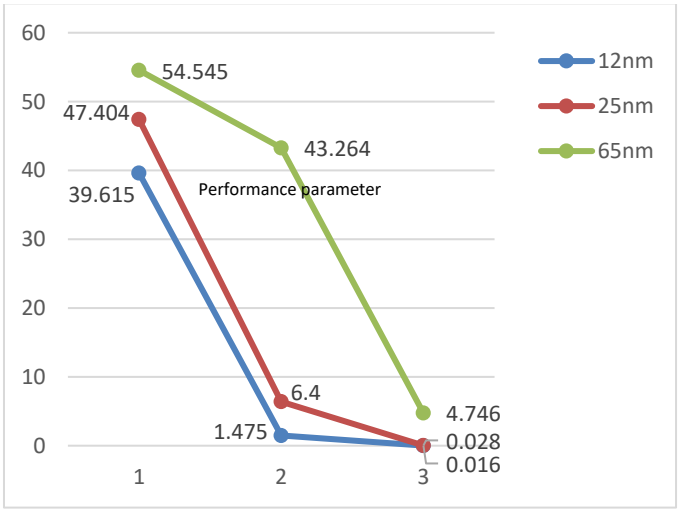
Table 3. Average Current Drawn for each technology node

Technology Node	Avg. Current Drawn
12	0.016 mA
25	0.028 mA
65	4.746mA

Table 4 Power consumed at each technology node

Technology Node	Power Consumed
12	39.615 µW
25	47.404 µW
65	54.545 µW

Figure 11 shows how each 4-bit CMOS full adder fares with each performance parameter. According to the chart setup, the lowest line would be the ideal candidate. Accordingly, 12nm technology displays the most desirable characteristics where the least amount of power (39.615 µW), least amount of average current (0.016mA) and least amount f Area is required (1.475 μm^2). It should be noted that the 4-bit Full Adder was tested at each node for a duration of 200ns. A long duration was necessary due to the complexity of the circuit and the time required for C_{out} to show a high state



1: Power Consumed, 2: Area Required, 3:Average Current

Fig 11: Comparative Line Chart

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5. CONCLUSION

These designs were tested at three different levels of CMOS technology: 12 nm, 25 nm, and 65 nm. The design

process is discussed in this work, as well as the simulations of the designs in the DSCH environment and the Microwind environment, respectively. Comparing the performance of various nodes, it has been have proved that the 12 nm technology node occupies the smallest amount of surface area. The circuit's average current and power usage are both at their lowest at this node [9]. Overall, this study aims to show how a 4-bit CMOS-based complete adder circuit is developed and simulated with Microwind and DSCH across several technology nodes. We then compare the results to see whether there is any correlation between the transistor size and the potential benefits. Afterwards. The purpose of this circuit is to implement a binary addition with four bits. The CMOS design process can be automated to the point that a full 4-bit adder can be created. The first CMOS design creates the idea and layout for a 4-bit complete adder. The designs are manufactured and simulated using technologies at the 90 nm, 65 nm, and 45 nm nodes. As shown by the results of simulations and the observed differences in the outputs of the two types of circuits, digital integrated circuits with smaller nodes perform better than those with larger nodes.

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