

Design and Performance Evaluation of Interleaved Marx Topology Boost Converter for High Gain DC-DC Conversion with Reduced Output Current Ripple

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ABSTRACT

The increasing power density of data centres has created a demand for efficient power conversion systems for computing and ICT loads. This paper presents a 4-stage Interleaved Marx Topology Boost Converter (IMTBC) for high-gain DC-DC conversion, focusing on improving current performance through interleaved switching. The converter converts 50 V to 800 V at 6 kW and 50 kHz. Its performance is evaluated against a Conventional Boost Converter (CBC) and a 4-stage Synchronized Marx Topology Boost Converter (SMTBC) using PLECS simulations. Results show that the IMTBC reduces output current ripple from 4.29 A in the SMTBC to 0.30 A, representing a 93% reduction, supporting its potential for HVDC data centre.

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1. INTRODUCTION

The increasing adoption of continuous computing, data storage, and networking services has driven the demand for high-density Information and Communication Technology (ICT) equipment, resulting in a rapid increase in data centre power consumption. In a conventional data centre, approximately 55% of the total energy consumption is associated with facility infrastructure, while the remaining 45% is consumed directly by ICT equipment such as servers, storage, and networking devices [1]. Among the facility loads, cooling systems account for approximately 40% of the total power consumption, followed by power feeding systems and lighting. This demand is expected to increase further with the deployment of high-performance computing and high-density server racks. In Malaysia, data centre electricity demand in Peninsular Malaysia is projected to increase from 7% of total electricity consumption in 2026 to 31% by 2035 [3]. This rapid growth highlights the need for more efficient and compact power delivery systems for data centre applications [10],[11],[12],[13],[14].

Conventional data centres commonly employ alternating current (AC) power distribution with uninterruptible power

supply (UPS) systems, which involve multiple power conversion stages between the utility supply and ICT loads [2]. In contrast, direct current (DC) distribution can reduce the number of conversion stages and associated conversion losses. The conventional 48 V DC distribution system used in ICT applications provides fewer conversion stages; however, supplying high-power and high-density ICT equipment at low voltage requires a large current. Consequently, larger power cables are required, increasing copper usage, cabling volume, and heat generation. Higher-voltage direct current (HVDC) distribution at approximately 380 V can significantly reduce the current required for the same power level. Previous studies have reported that the volume of copper required for a 380 V HVDC system can be substantially lower than that of a 48 V DC system [4]. Therefore, HVDC distribution is a promising approach for supporting the increasing power density of modern data centres [6]-[9],[16],[18],[19].

In addition to efficiency and voltage conversion capability, the physical size of power conversion equipment has become an important consideration in high-density data centre systems. Recent specifications for high-density computing applications require power converters to process several kilowatts within a

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highly compact form factor. For example, a 6-kW converter with a footprint of 70 mm × 60 mm and a height of 11 mm corresponds to a power density of approximately 2130 W/in³ [5]. Therefore, future data centre power converters must achieve high voltage conversion ratios and efficiency while minimizing passive component size, semiconductor stress, and overall converter volume [12],[15],[20].

These requirements create a need for compact DC-DC converter topologies capable of providing high voltage gain from low-voltage sources to the 380–400 V HVDC bus. Conventional boost converters provide step-up operation, however, achieving a high conversion ratio from a low-voltage source to a 380–400 V bus can result in high component stress and demanding operating conditions. Integrating the boost structure with a multistage Marx topology can increase the voltage gain through capacitor-based voltage multiplication without relying solely on a very wide duty cycle. However, the switching technique significantly influences the converter performance. Synchronized switching provides a simple and coordinated operation of the Marx stages, but it can result in higher input and output current ripple. In contrast, interleaved switching introduces phase shifts between the switching stages, enabling better current distribution and reduced current ripple. Therefore, an improved topology is required to achieve high voltage gain operation while maintaining low current ripple, reduced component stress, and high-power density. In this work, a Marx topology boost converter is proposed for 380–400 V HVDC data centre power distribution. The proposed converter aims to provide high voltage gain while improving the suitability of the converter for compact, high-power-density data centre applications [21], [22], [23], [24], [26], [27], [29], [30], [32]–[40], [42]–[47], [55], [56].

2. THEORETICAL PRINCIPLE

This section discusses the high voltage gain principle, multilevel and modular structure and output current ripple variation as a function of switching frequency.

2.1 High Voltage Gain Principle

Fig. 1. shows how output voltage (V_{out}) changes with duty cycle (D) for three types of boost converters. The Conventional Boost Converter (CBC) has the lowest voltage gain. It rises slowly at low to medium duty cycles and needs a very high duty cycle of $D = 0.94$ to reach 800 V. Operating at such a high duty cycle is not practical in real life because it forces the switch to turn off in a very short time, causing severe switch stress, high power losses, and poor efficiency [21], [29], [30], [33], [44], [46], [55].

In contrast, Synchronized Marx Topology Boost Converter (SMTBC) is able to significantly boost the output voltage. The SMTBC gives the highest output voltage across the whole range, reaching 818 V at a much lower duty cycle of $D \approx 0.81$ [24], [26], [35], [36], [42], [45].

The Interleaved Marx Boost Converter (IMTBC) applies an interleaved switching technique to reduce output current ripple. While its voltage starts lower than the CBC, its voltage rises quickly as D increases, passing the CBC and reaching an output voltage of 816 V at $D = 0.84$ [22], [34], [39], [43], [58]–[60].

Overall, both SMTBC and IMTBC reach the high voltage gain at much lower duty cycles than the CBC. Operating at lower duty cycles avoids driving the converter to extreme limits which keeps the switches cooler, reduces stress on parts, and makes the system work much better.

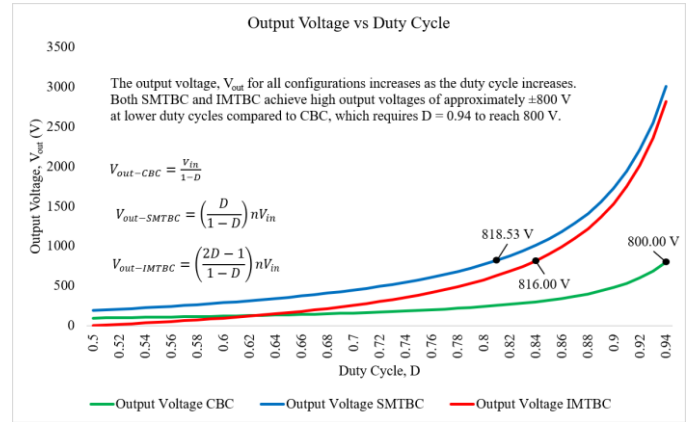


Fig. 1. Output Voltage vs Duty Cycle

2.2 Multilevel and Modular Structure

Fig. 2. shows the circuit of CBC. The CBC is not suitable for high voltage and high-power applications as the current drawn by the input converter will be high. As a result, the current flowing through the inductor is high and causing increased current stress in the inductor. Fig. 2. demonstrates that the inductor is connected in series with the input source. In this case, the current flow through the inductor is same as the input current of the converter [21], [29], [30], [35], [46].

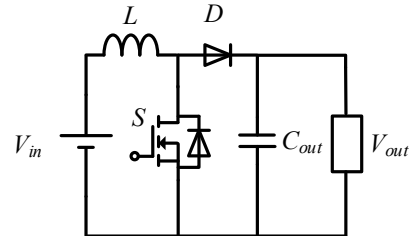


Fig. 2. Conventional Boost Converter (CBC)

Fig. 3 shows the modular structure of Marx Topology Boost Converter (MTBC). The MTBC improves the voltage conversion capability by combining multiple Marx modules to form a multilevel converter structure. It consists of several capacitors and switching devices as spark gaps. During the charging stage, the capacitors are charged in parallel to the supply voltage. When the switches are triggered, the capacitors are effectively connected in series, causing their individual voltages to add together and produce a much higher output voltage [17], [23], [24], [37], [38], [47], [49], [50], [52]–[54].

Unlike the conventional boost converter (CBC), where the input source is connected to a single inductor and the entire input current flows through one switching path, the MTBC distributes the input current among multiple parallel-connected stages. For an n -stage MTBC, the total input current is shared among the n input stages, such that the average current handled by each stage is approximately reduced on each stage under balanced operating conditions. Consequently, the current stress experienced by each input inductor and switching device is significantly lower than that of the CBC at the same power level. This current-sharing characteristic is particularly

beneficial for high-power applications, where a large input current can result in increased conduction losses, magnetic component size, and electrical stress. In addition, the modular arrangement allows the voltage gain to be increased through the cascading of multiple stages without requiring the converter to operate at an extremely high duty cycle. Therefore, the MTBC provides both high voltage gain and improved current handling capability, making it more suitable for high-power, high voltage DC applications [23], [24], [37], [38], [47]-[50], [52]-[54], [56], [57].

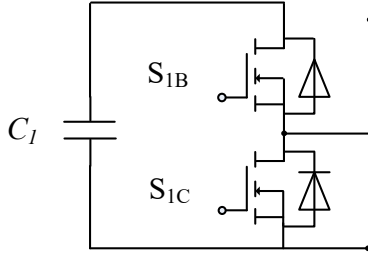


Fig. 3. MTBC modular structure

2.3 Current Ripple Variation with Switching Frequency

By applying an interleaved switching technique to the primary switches, Switch A across the converter stages, the gate control signals are phase-shifted by half switching cycle of the switching period. Switch A operates at the fundamental switching frequency, f_{sw} to manage energy storage within the input inductors. Conversely, the secondary auxiliary switches, Switch B and Switch C, controls the charging and discharging of the capacitors, operating inversely from primary switches, Switch A. The two phases interleaved by Switch A causing switch B and C to occur twice within each switching period thereby doubling their effective operating frequency to $2f_{sw}$. As the Switch A operate at switching frequency, f_{sw} is 50 kHz, switch B and C operate at 100 kHz. Fig. 4. shows the relationship between the current ripple and switching frequency. This demonstrates that the output current ripple of the converter decreases as the switching frequency increases [22], [34], [39], [43], [58]-[60].

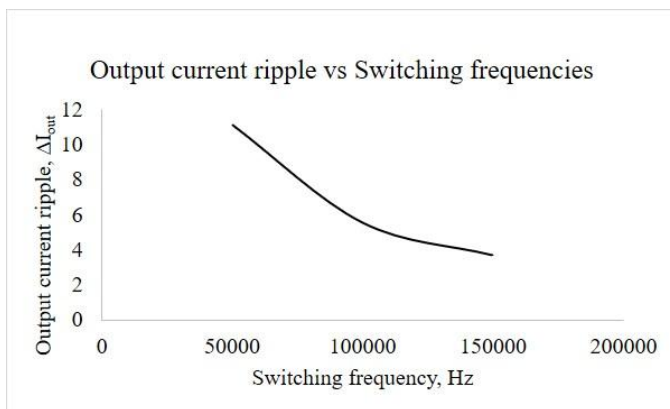


Fig. 4. Current ripple vs switching frequency

3. CONVERTER CONFIGURATION

This section will discuss about circuit structure, switching strategy and parameter design of the interleaved Marx Topology Boost Converter.

3.1 Circuit Structure

Fig. 5. shows the 4-stage of MTBC circuit structure. Each stage consists of an inductor, diode, stage capacitor and 3 set of switches which are S_A , S_B and S_C . The input source V_{in} will be a low voltage source such as battery or solar panel. On the output side, an inductor and capacitor are placed to filter the output voltage and current for the suitable loads [25], [28], [32].

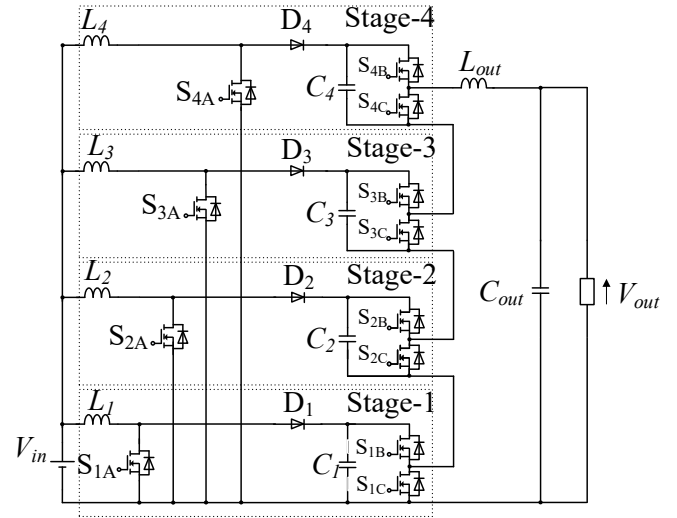


Fig. 5. MTBC circuit structure

3.2 Interleaved Switching Strategy

Interleaved switching techniques in 4-stage MTBC is defined as stage 1 and stage 2 operated alternately with stage 3 and stage 4. By using the interleaved switching techniques, the inductance values are reduced due to the increasing of equivalent frequency at the output side [22], [34], [43], [59], [60].

Fig. 6. shows the switching techniques of IMTBC. S_{1A} , S_{2A} , S_{3A} and S_{4A} is the main switch of the converter where S_{3A} and S_{4A} are phase-shifted by half a switching cycle from S_{1A} and S_{2A} . S_C is the inverse of S_{1A} and S_{2A} , while S_B is the inverse of S_C . The output side switches group which are S_B and S_C has a twice of the equivalent frequency of the input side switches group.

For a converter system operating at a duty cycle of 0.80 and a switching frequency of 50kHz, the switching period is 20 μ s. Accordingly, $D\alpha$ occurs at 10 μ s, followed by $D\beta$ at 10.2 μ s and $D\omega$ is 14.3 μ s. Since this converter considering dead-time and delay to avoid short circuit and surge voltage of the switches, where $DT\beta$ is 0.2 μ s and $DT\omega$ is 0.1 μ s.

Interleaved switching techniques consist of 12 operation modes. The stage capacitors $C1$ and $C2$ are charging together at the same time meanwhile $C3$ and $C4$ is charging alternately. All the capacitors discharged simultaneously Therefore, within one cycle of interleaved switching techniques, the stage capacitors undergo charging and discharging twice. As a result, the equivalent frequency at the output side is doubled of the switching frequency, achieving the high boost ratio.

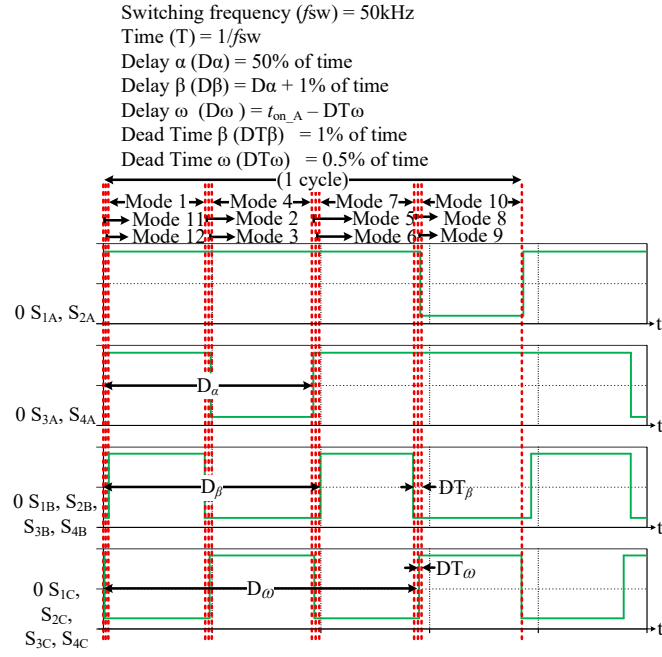


Fig. 6. Interleaved switching techniques

From switching scheme shown in Fig. 6., the capacitor charging and discharging behaviour can be identified as in Table 1.

Table 1. Stage capacitors operation on 4-stage MTBC

Mode	Switches				Capacitor	
	S _{1A} , S _{2A}	S _{3A} , S _{4A}	S _B	S _C	C ₁ , C ₂	C ₃ , C ₄
1	ON	ON	ON	OFF	Discharging	
2	ON	ON	OFF	OFF	Dead time	
3	ON	ON	OFF	ON	Delay	
4	ON	OFF	OFF	ON	Charge	Discharge
5	ON	ON	OFF	ON	Delay	
6	ON	ON	OFF	OFF	Dead time	
7	ON	ON	ON	OFF	Delay	
8	ON	ON	OFF	OFF	Dead time	

9	ON	ON	OFF	ON	Delay	
10	OFF	ON	OFF	ON	Discharge	Charge
11	ON	ON	OFF	ON	Delay	
12	ON	ON	OFF	OFF	Dead time	

3.3 Parameter Design

The simulation will compare the result between synchronized and interleaved switching techniques. The output voltage of Synchronized Marx Topology Boost Converter (SMTBC) and Interleaved Marx Topology Boost Converter (IMTBC) can be determined as follows:

$$V_{out} = \left(\frac{D_{SMTBC}}{1-D_{SMTBC}} \right) nV_{in} \quad (1)$$

$$V_{out} = \left(\frac{2D_{IMTBC}-1}{1-D_{IMTBC}} \right) nV_{in} \quad (2)$$

The resistor load for each simulation of SMTBC and IMTBC can be expressed as follows:

$$R = \frac{V_{out}^2}{P_{out}} \quad (3)$$

The minimum inductor for the converter to operate at continuous conduction mode (CCM) can be determined using the following formula:

$$L_{in(m)} > \frac{n(V_{in})^2 D}{2P_{out}f_{sw}} \quad (4)$$

The relationship between inductor current ripple and input inductor current can be investigated using the formula below:

$$\Delta I_{Lin(m)} = \frac{V_{in}D}{f_{sw}L_{in(m)}} \quad (5)$$

The average of input inductor current on each stage can be calculated as follows:

$$I_{L(m)-avg} = \frac{P_{in}}{nV_{in}} \quad (6)$$

The inductance of output inductor can be determined using the following formula:

$$L_{out} = \frac{\left(\frac{V_{in}}{1-D} - V_{out} \right) D}{f_{sw}\Delta I_{Lout}} \quad (7)$$

The capacitance of each stage capacitor can be formulated as follows:

$$C_{(m)} = \frac{I_{L-ave(m)}(1-D)}{\Delta V_{C(m)}f_{sw}} = \frac{P_{in}(1-D)}{nV_{in}\Delta V_{C(m)}f_{sw}} \quad (8)$$

The maximum stage capacitor voltage is calculated to ensure it does not exceed the drain source voltage of the switching devices using the following formula:

$$V_{C(m)-max} = V_{DS-max} = V_{in} + \frac{V_{out}}{n} \quad (9)$$

4. SIMULATION SETUP

The proposed converters were modelled and simulated using PLECS software. The design specifications are summarized in Table 2.

Table 2. Simulation specifications

Specifications	Value
Input voltage, V_{in}	48 V
Output voltage, V_{out}	300 V
Output power, P_{out}	600 W
Switching frequency, f_{sw}	50 kHz
Input inductance, L_{in}	500 μ H
Output inductance, L_{out}	650 μ H
Stage capacitors, C_{in}	44 μ F
Output capacitor, C_{out}	50 μ F
Resistance, R	150 Ω

The simulation results obtained from the developed model are presented and discussed in the subsequent section to verify the voltage boosting capability, switching behaviour, and overall performance of the proposed IMTBC.

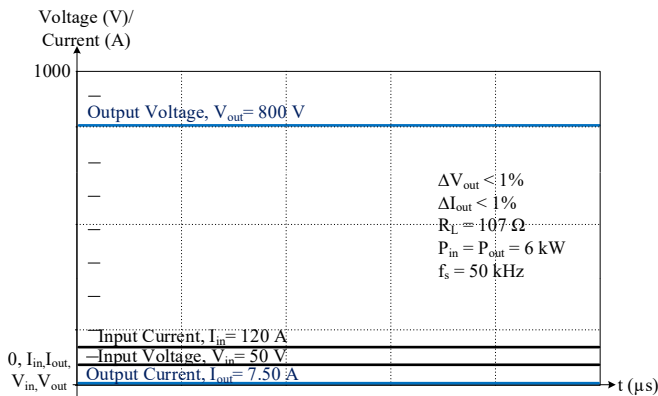


Fig. 7. Key performance waveform of the converter

Fig. 7. illustrates the key performance waveform of the steady state behaviour of the converter where the input voltage is set to 50 V to get an output of 800 V with output power 6kW. The current and voltage ripple tolerance is set at 1% and 1% respectively.

5. RESULTS AND DISCUSSIONS

This section discusses about the simulation results comparing Conventional Boost Converter (CBC), SMTBC and IMTBC. The discussion will include current stress, current ripple, and voltage stress of the converters.

5.1 Input Inductor Current Stress

The MTBC multilevel structure demonstrates that parallel inductor configuration effectively distributes the current stress among the stages. The stress is significantly reduced by approximately 75%, decreasing from 120 A to 30 A, as illustrated in Fig. 8.

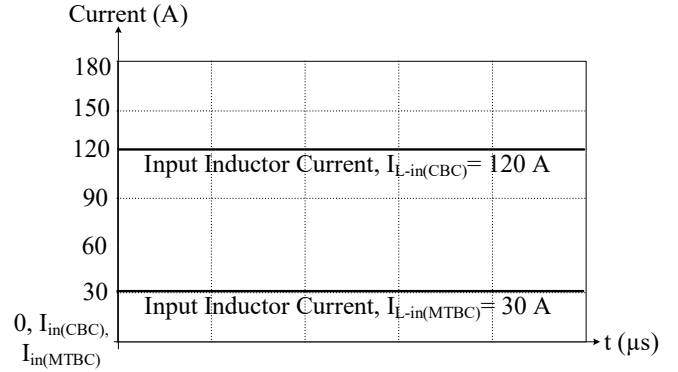
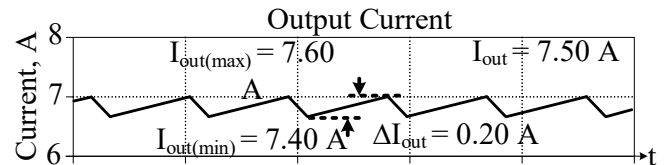


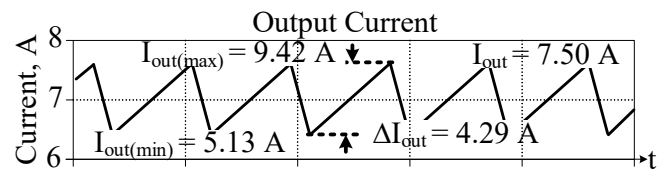
Fig. 8. Input inductor current stress

5.2 Output Current Ripple

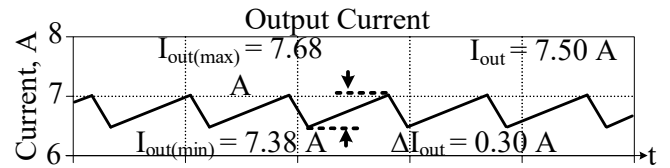
Fig. 9. shows a comparison of the output current ripple among the CBC, SMTBC, and IMTBC. Fig. 9. (a) shows the desired output current ripple of CBC at 0.20 A while Fig. 9. (b) shows the output current ripple increased to 4.29 A. After implementing interleaved switching techniques, the output current ripple of MTBC achieved the same desired ripple level as CBC. The reduced current ripple highlights the effectiveness of the proposed converter in supporting sensitive loads, including data centre equipment, GPUs, CPUs, and artificial intelligence (AI) computing applications.



(a)



(b)



(c)

Fig. 9. Output current ripple of (a) CBC (b) SMTBC and (c) IMTBC

5.3 Switching Devices Voltage Stress

Principally, the voltage stress on switching device of CBC is equal to the output voltage produced by the converter. The simulation results of voltage stress on CBC proved that the CBC suffered high voltage stress on switching device as shown in Fig. 10. It indicated that when the converter produced an output voltage of 800 V, the maximum voltage across switching device which is a drain-source voltage of the MOSFET is 800 V. The drain-source voltage of the MOSFET increase according to the increasing the output voltage of the converter. A high voltage rating of switching device needs to be considered so that the switching device can withstand the output voltage of CBC.

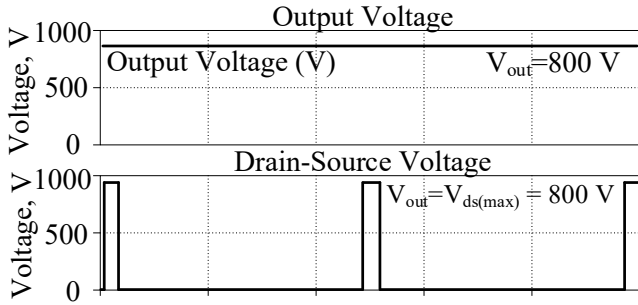


Fig. 10. Voltage stress on switching device of CBC

With the intention to reduce the voltage stress on the switching device of CBC, the simulation continue to test the reliability of MTBC structure in reducing the voltage stress on switching device. The result of voltage stresses on switching devices of SMTBC is shown in Fig. 11. The SMTBC reduces the switch voltage stress by approximately 68.75% compared to the CBC. Consequently, the SMTBC provides the better reduction in switch voltage stress and allow converter to use lower rating of switching devices.

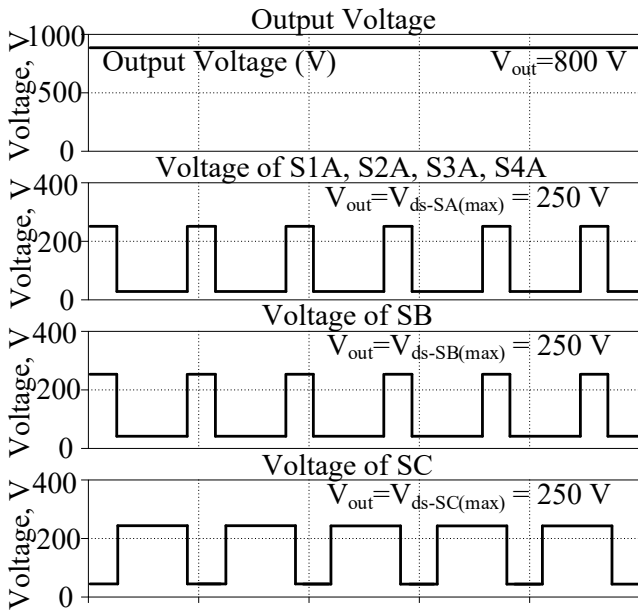


Fig. 11. Voltage stress on switching device of SMTBC

As illustrated in Fig. 12, the switching devices in the IMTBC configuration are subjected to a voltage stress of 300 V each,

while the SMTBC switches experience a significantly reduced stress of 250 V. Compared to the CBC, the MTBC lowers the voltage stress on each switching device by introducing auxiliary switches, SB and SC to distribute the stress evenly.

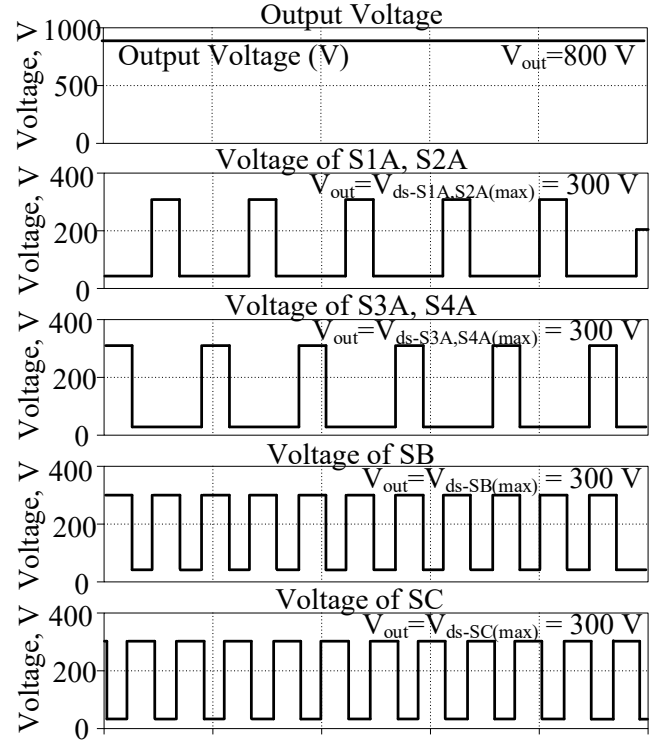


Fig. 12. Voltage stress on switching device of IMTBC

5.4 Capacitor Voltage Balancing

Fig. 13. presents a steady-state performance comparison of stage capacitors voltage of SMTBC and IMTBC operating under identical conditions. Both topologies maintain a constant output voltage, V_{out} of 800 V over time. However, the stage capacitor voltage stress differs significantly between the two structures as the capacitor in the IMTBC operates at a higher voltage level of 300 V represented by the red line, whereas the capacitor in the SMTBC experiences a lower voltage stress of 250 V represented by the blue line. This lower voltage stress in the SMTBC topology is advantageous because it allows the use of lower-voltage-rated components, which typically offer smaller physical sizes, lower manufacturing costs, and higher overall system conversion efficiency.

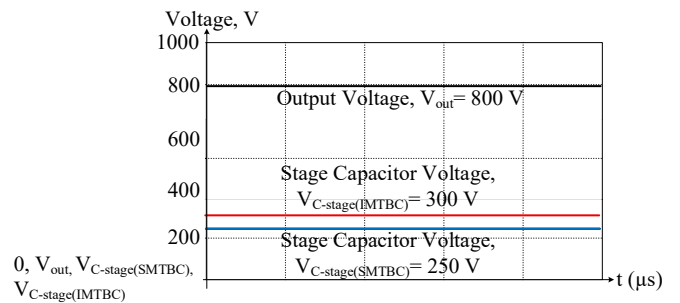


Fig. 13. Capacitor voltage on each stage of SMTBC and IMTBC

5.5 Inductor Current Sharing

Fig. 14. shows the inductor current sharing between each stage of input inductors. The average current of each stage inductor is reduced by a factor of four due to the four parallel-connected input stages. As the number of interleaved stages increases, the input current is distributed among the corresponding inductors, resulting in a proportional reduction of the current stress on each inductor. Consequently, the conduction losses and copper losses are reduced, improving the overall efficiency and thermal performance of the converter.

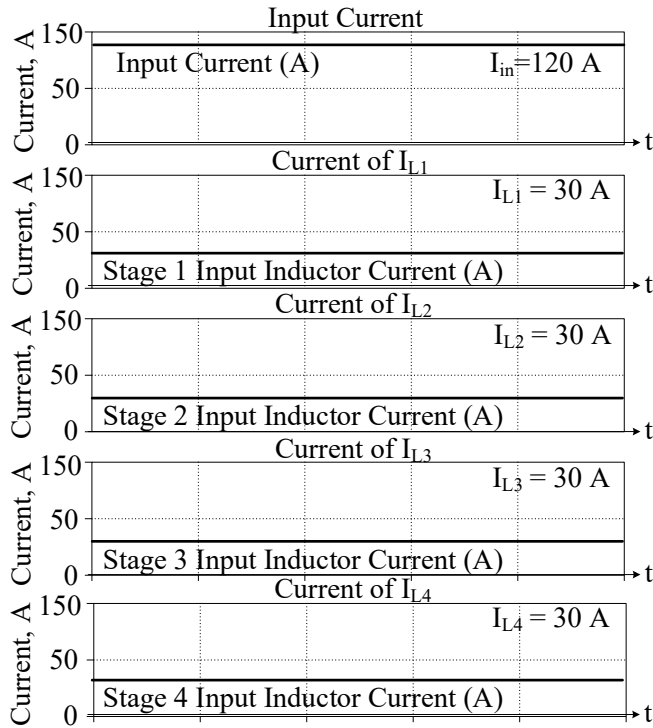


Fig. 14. Inductor current on each stage of MTBC

5.6 Overall Performance Comparison

The performance comparison across the three converter topologies CBC, SMTBC and IMTBC reveals significant operational deviations across current stress, voltage stress, and output ripple performance. As shown in Fig. 15., both the IMTBC ($D=0.833$) and SMTBC ($D=0.800$) achieved 75% reduction in input inductor current stress compared to the traditional CBC, effectively minimizing conduction losses (I^2R).

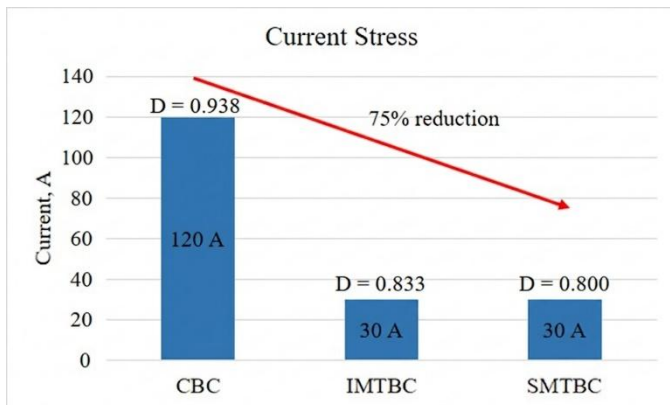


Fig. 15. Significant finding regarding reduction of current stress on input inductor

Furthermore, Fig. 16. demonstrates that the SMTBC topology provides the lowest semiconductor voltage stress at 250 V, marking 68.75% reduction from the CBC's full output stress of 800 V, which enables the selection of lower-voltage-rated MOSFETs to boost overall system efficiency.

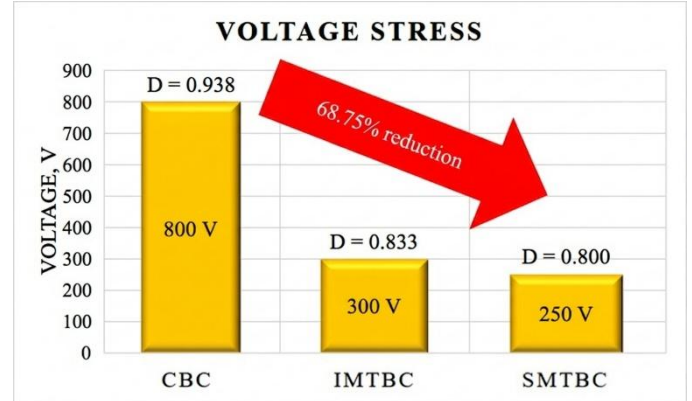


Fig. 16. Key outcome regarding reduction of voltage stress on switching devices

Finally, Fig. 17. highlights that while the SMTBC experiences a slightly higher output current ripple of 4.29 A, the IMTBC topology achieves better ripple reduction capability with a lower ripple of 0.3 A, presenting a design variation of ripple reduction and component stress minimization.

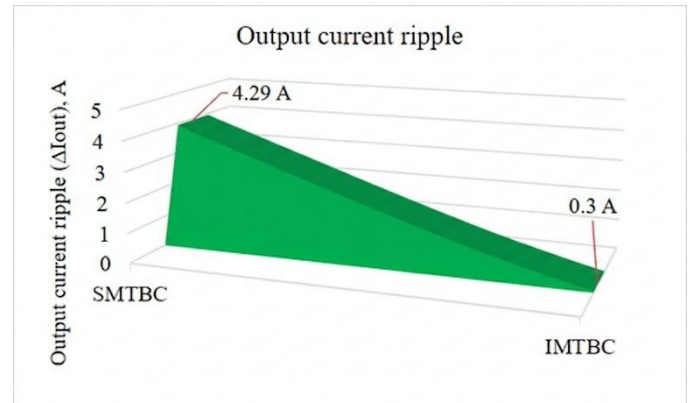


Fig. 17. Principal outcome on reduction of output inductor current ripple

5.7 Future Converter Extensions

The successful implementation of interleaving in the MTBC suggests that the Marx capacitor charging and discharging concept may be extended to other converter structures. Potential future research directions include Marx-assisted buck converters, buck-boost converters, flyback converters, SEPIC converters, and isolated converter topologies.

Further investigation into Automatic Voltage Regulation (AVR), Automatic Current Regulation (ACR), and digital control strategies may also improve converter dynamic performance.

1. CONCLUSION

This paper has presented the analysis and performance evaluation of the proposed interleaved Marx topology-based converter (IMTBC), with particular focus on input and output current ripple characteristics as well as current and voltage stress distribution among components. The results demonstrate that the interleaved switching strategy significantly improves the input current behaviour, enabling the IMTBC to achieve a ripple level comparable to that of a conventional boost converter, while the SMTBC fails to achieve similar performance. Quantitatively, the IMTBC achieves a 93% reduction in output current ripple relative to the SMTBC, highlighting the effectiveness of the interleaving technique in mitigating source-side current ripples.

In addition, the multilevel MTBC structure with parallel inductor configuration is shown to effectively distribute current stress across the converter components. This configuration leads to a significant reduction in current stress, decreasing from 120 A to 30 A, corresponding to an improvement of approximately 75%. Such a reduction is particularly beneficial for enhancing converter efficiency, reducing component stress, and improving overall system lifetime.

A detailed performance analysis reveals that SMTBC offers the lowest switch voltage stress of 250 V, representing a 68.75% reduction compared to CBC. Meanwhile, the proposed IMTBC excels in output power quality, successfully minimizing output current ripple compared to the other topologies. Specifically, the IMTBC operates at a moderate duty cycle $D = 0.833$ vs $D = 0.938$ for CBC while delivering better ripple reduction capability, reducing the output current ripple to 0.30 A compared to 4.29 A in the SMTBC.

Furthermore, frequency analysis confirms that increasing switching frequency significantly decreasing output ripple, allowing a reduction in magnetic component size. Overall, the IMTBC provides a balanced solution combining lower duty cycle operation, reduced switch voltage stress and exceptional output current quality, making it highly suitable for powering sensitive loads such as GPUs, CPUs, and AI computing hardware.

Future work will focus on extending the proposed IMTBC topology toward higher power levels and experimental hardware validation to complement the simulation results. Further investigation will also consider efficiency optimization under wide load and duty-cycle variations, as well as the impact of non-ideal component characteristics such as parasitic inductance and capacitance. In addition, advanced control strategies, including digital current-mode control and adaptive interleaving techniques, will be explored to further enhance dynamic performance and improve robustness under transient operating conditions.

REFERENCES

- [1] K. Asakura, T. Tanaka, and T. Babasaki, "Higher-voltage direct current power-feeding system," *NTT Technical Review*, vol. 9, no. 2, pp. 1–6, 2011. doi: <https://doi.org/10.53829/ntr201102fa2>.
- [2] Y. Nozaki, "Development of higher-voltage direct current power feeding system for ICT equipment," *NTT Technical Review*, vol. 7, no. 10, pp. 1–5, 2009. doi: <https://doi.org/10.53829/ntr200910sf2>.
- [3] L. Hakim and M. Al As, "Data centre power demand in Peninsular Malaysia to surge to 31pct by 2035," *New Straits Times*, Jul. 1, 2026. url: <https://www.nst.com.my/amp/news/nation/2026/07/1477411/data-centre-power-demand-peninsular-malaysia-surge-31pct-2035>
- [4] A. Fukui, T. Takeda, K. Hirose, and M. Yamasaki, "HVDC power distribution systems for telecom sites and data centers," in *Proc. 2010 Int. Power Electronics Conf. (IPEC-ECCE ASIA)*, Sapporo, Japan, 2010, pp. 874–880. doi: <https://doi.org/10.1109/IPEC.2010.5543344>.
- [5] P. R. Prakash and Q. Li, "High-density, high-efficiency GaN-based 800 V/50 V LLC converter for future datacenters," in *Proc. 2026 IEEE Applied Power Electronics Conf. and Expo. (APEC)*, 2026, pp. 2790–2797. doi: <https://doi.org/10.1109/APEC51134.2026.11517167>.
- [6] T. Tanaka et al., "HVDC power supply system implementation," *NTT Tech. Rev.*, vol. 13, no. 3, pp. 1–7, 2015. doi: <https://doi.org/10.53829/ntr201503fa7>.
- [7] M. Matsuoka, "Energy and environment R&D toward environmental impact reduction," *NTT Tech. Rev.*, vol. 7, no. 10, pp. 1–8, 2009. doi: <https://doi.org/10.53829/ntr200910sfl>.
- [8] T. Tanaka, K. Asakura, and T. Babasaki, "Trends in the international standardization of HVDC power feeds," *NTT Tech. Rev.*, vol. 11, no. 3, pp. 1–6, 2013. doi: <https://doi.org/10.53829/ntr201303gls>.
- [9] Y. Udagawa and H. Matsuo, "Power supply technology and air conditioning technology for ICT," *NTT Tech. Rev.*, vol. 12, no. 11, pp. 1–8, 2014. doi: <https://doi.org/10.53829/ntr201411fa10>.
- [10] H. Hoshi et al., "Development of equipment for HVDC power supply systems," *NTT Tech. Rev.*, vol. 13, no. 3, pp. 1–5, 2015. doi: <https://doi.org/10.53829/ntr201503fa8>.
- [11] V. A. Prabhala, B. P. Baddipadiga, P. Fajri, and M. Ferdowsi, "An overview of direct current distribution system architectures & benefits," *Energies*, vol. 11, no. 9, Art. no. 2463, 2018. doi: <https://doi.org/10.3390/en11092463>.
- [12] H. Huang, W. Lin, J. Lin, and K. Li, "Power management optimization for data centers: A power supply perspective," *IEEE Trans. Sustain. Comput.*, vol. 10, no. 4, pp. 1–20, 2025. doi: <https://doi.org/10.1109/TSUSC.2025.3542779>.
- [13] X. Chen, X. Wang, A. Colacelli, M. Lee, and L. Xie, "Electricity demand and grid impacts of AI data centers: Challenges and prospects," 2025, *arXiv:2509.07218*. doi: <https://doi.org/10.48550/arXiv.2509.07218>.
- [14] T. Tanaka et al., "Energy-distribution platform technologies toward zero environmental impact," *NTT Tech. Rev.*, vol. 19, no. 6, pp. 1–8, 2021. doi: <https://doi.org/10.53829/ntr202106fa3>.
- [15] S. Chen, G. Zhang, S. S. Yu, Y. Mei and Y. Zhang, "A Review of Isolated Bidirectional DC-DC Converters for Data Centers," in *Chinese Journal of Electrical Engineering*, vol. 9, no. 4, pp. 1–22, December 2023. doi: <https://doi.org/10.23919/CJEE.2023.000034>.
- [16] D. J. Becker and B. J. Sonnenberg, "400Vdc power distribution: Overcoming the challenges," *Intelec 2010*, Orlando, FL, USA, 2010, pp. 1–10. doi: <https://doi.org/10.1109/INTELEC.2010.5525660>.
- [17] A. B. Ponnirani and M. A. N. B. Kasiran, "Parameters design evaluation in 3-level flying capacitor boost converter," *2017 IEEE Symposium on Computer Applications & Industrial Electronics (ISCAIE)*, Langkawi, Malaysia, 2017, pp. 195–199. doi: <https://doi.org/10.1109/ISCAIE.2017.8074976>.
- [18] M. Noritake, K. Hirose, M. Yamasaki, T. Oosawa and H. Mikami, "Evaluation results of power supply to ICT equipment using HVDC distribution system," *Intelec 2010*, Orlando, FL, USA, 2010, pp. 1–8. doi: <https://doi.org/10.1109/INTELEC.2010.5525651>.
- [19] T. Tanaka et al., "The HVDC power supply system implementation in NTT group and next generation power supply system," *2014 IEEE 36th International Telecommunications Energy Conference (INTELEC)*, Vancouver, BC, Canada, 2014, pp. 1–6. doi: <https://doi.org/10.1109/INTELEC.2014.6972160>.
- [20] A. Matsumoto, A. Fukui, T. Takeda and M. Yamasaki, "Development of 400-Vdc output rectifier for 400-Vdc power distribution system in telecom sites and data centers," *Intelec 2010*, Orlando, FL, USA, 2010, pp. 1–6. doi: <https://doi.org/10.1109/INTELEC.2010.5525652>.
- [21] E. Babaei, A. Mofidi, and S. Laali, "Calculation of switching current stress in high voltage gain boost DC-DC converter," in *Proc. IEEE Int. Conf. Electr. Syst. Aircraft, Railway, Ship Propulsion Road Vehicles (ESARS)*, Aachen, Germany, 2015, pp. 1–6. doi: <https://doi.org/10.1109/ESARS.2015.7101516>.

- [22] M. Muhammad, M. Armstrong, and M. A. Elgendy, "A non-isolated interleaved boost converter for high-voltage gain applications," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 2, pp. 677–680, Jun. 2016. doi: <https://doi.org/10.1109/JESTPE.2015.2488839>.
- [23] M. A. Perez, S. Bernet, J. Rodriguez, S. Kouro, and R. Lizana, "Circuit topologies, modelling, control schemes and applications of modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 4–17, Jan. 2015. doi: <https://doi.org/10.1109/TPEL.2014.2310127>.
- [24] Y. Li, X. Lyu, and D. Cao, "A high voltage gain modular multilevel DC-DC converter," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Montreal, QC, Canada, 2015, pp. 3535–3541. doi: <https://doi.org/10.1109/ECCE.2015.7310160>.
- [25] T. S. Anandhi and S. PremKumar, "Application of DC-DC boost converter for solar powered traffic light with battery backup," *Indian J. Sci. Technol.*, vol. 8, no. 32, pp. 1–5, Nov. 2015. doi: <https://doi.org/10.17485/jst/2015/v8i1/84408>.
- [26] V. A. K. Prabhala, P. Fajri, V. S. P. Gouribhatla, B. P. Baddipadiga, and M. Ferdowsi, "A DC–DC converter with high voltage gain and two input boost stages," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4206–4215, Jun. 2016. doi: <https://doi.org/10.1109/TPEL.2015.2476377>.
- [27] P. K. Maroti, M. S. B. Ranjana, and D. K. Prabhakar, "A novel high gain switched inductor multilevel buck-boost DC-DC converter for solar applications," in *Proc. IEEE 2nd Int. Conf. Electr. Energy Syst. (ICEES)*, Chennai, India, 2014, pp. 152–156. doi: <https://doi.org/10.1109/ICEES.2014.6924159>.
- [28] I. Alhamrouni, W. I. Hanis, M. Salem, F. M. Albatsh, and B. Ismail, "Application of DC-DC converter for E.V battery charger using PWM technique and hybrid resonant," in *Proc. IEEE 6th Int. Conf. Power Energy (PECON)*, Melaka, Malaysia, 2016, pp. 133–138. doi: <https://doi.org/10.1109/PECON.2016.7951547>.
- [29] R. Davis, "Developed non-isolated high step-up converter with low voltage stress," M.S. thesis, Dept. Electr. Comput. Eng., Univ. Akron, Akron, OH, USA, 2016. url: <https://ideaexchange.uakron.edu/gradspace/185/>
- [30] C. Srideepa, S. S. Kumar, and R. Nagarajan, "High gain and reduced switch stress DC-DC converter topology for PV system," *Int. J. Pure Appl. Math.*, vol. 119, no. 15, pp. 23808–23816, 2018.
- [31] N. Bianchi and M. Dai Pre, "Active power filter control using neural network technologies," *IEE Proc. - Electr. Power Appl.*, vol. 150, no. 2, pp. 139–145, Mar. 2003.
- [32] Y. Zhang, J. Liu, X. Ma, and J. Feng, "Comparison of conventional DC-DC converter and a family of diode-assisted DC-DC converter in renewable energy applications," *J. Power Electron.*, vol. 14, no. 2, pp. 203–216, Mar. 2014. doi: <https://doi.org/10.6113/JPE.2014.14.2.203>.
- [33] B. P. Baddipadiga, "High-voltage-gain DC-DC power electronic converters -- New topologies and classification," Ph.D. dissertation, Dept. Electr. Comput. Eng., Missouri Univ. Sci. Technol., Rolla, MO, USA, 2016. url: https://scholarmine.mst.edu/doctoral_dissertations/2529/
- [34] M. A. Harimon, A. Ponnirani, A. N. Kasiran, and H. H. Hamzah, "A study on 3-phase interleaved DC-DC boost converter structure and operation for input current stress reduction," *Int. J. Power Electron. Drive Syst.*, vol. 8, no. 4, pp. 1948–1953, Dec. 2017. doi: <https://doi.org/10.11591/ijpeds.v8.i4.pp1948-1953>.
- [35] J.-J. Yun, "A new dual boost DC/DC converter with a high voltage gain," *Indian J. Sci. Technol.*, vol. 9, no. 17, pp. 1–6, May 2016. doi: <https://doi.org/10.17485/jst/2016/v9i17/92303>.
- [36] W. Qian, D. Cao, J. G. Cintron-Rivera, M. Gebben, D. Wey, and F. Z. Peng, "A switched-capacitor DC-DC converter with high voltage gain and reduced component rating and count," *IEEE Trans. Ind. Appl.*, vol. 48, no. 4, pp. 1397–1406, Jul./Aug. 2012.
- [37] J. C. Rosas-Caro, J. M. Ramirez, F. Z. Peng, and A. Valderrabano, "A DC–DC multilevel boost converter," *IET Power Electron.*, vol. 3, no. 1, pp. 129–137, Jan. 2010. doi: <https://doi.org/10.1049/iet-pel.2008.0253>.
- [38] M. Prudente, L. L. Pfitscher, G. Emmendoerfer, E. F. Romaneli, and R. Gules, "Voltage multiplier cells applied to non-isolated DC-DC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 871–887, Mar. 2008. doi: <https://doi.org/10.1109/TPEL.2007.915762>.
- [39] J. Liu and W. Wang, "High power high voltage gain interleaved DC-DC boost converter," in *Proc. IEEE Conf. Ind. Electron. Appl. (ICIEA)*, Beijing, China, 2010, pp. 1205–1209.
- [40] J. Dawidziuk, "Review and comparison of high efficiency high power boost DC/DC converters for photovoltaic applications," *Bull. Polish Acad. Sci. Tech. Sci.*, vol. 59, no. 4, pp. 499–506, Dec. 2011. doi: <https://doi.org/10.2478/v10175-011-0061-7>.
- [41] H.-M. Fischer and L. Dorn, "Voltage classes for electric mobility," German Electrical and Electronic Manufacturers' Assoc. (ZVEI), Frankfurt, Germany, Tech. Rep., 2013. url: <https://www.zvei.org/>
- [42] F. Mohammadzadeh Shahir, E. Babaei, M. Sabahi, and S. Laali, "A new DC–DC converter based on voltage-lift technique," *Int. Trans. Electr. Energy Syst.*, vol. 26, no. 6, pp. 1260–1286, Jun. 2016. doi: <https://doi.org/10.1002/etep.2133>.
- [43] G. A. L. Henn, R. N. A. L. Silva, P. P. Praça, L. H. S. C. Barreto, and D. S. Oliveira, "Interleaved-boost converter with high voltage gain," *IEEE Trans. Power Electron.*, vol. 25, no. 11, pp. 2753–2761, Nov. 2010. doi: <https://doi.org/10.1109/TPEL.2010.2049379>.
- [44] D. W. Hart, *Introduction to Power Electronics*. Upper Saddle River, NJ, USA: Prentice-Hall, 1997.
- [45] B. S. Satish and S. Jain, "High gain efficient DC-DC converter for low-voltage power generation application," in *Proc. IEEE Students' Conf. Electr. Electron. Comput. Sci. (SCEECS)*, Bhopal, India, 2016, pp. 1–5. doi: <https://doi.org/10.1109/SCEECS.2016.7509353>.
- [46] M. Saleem, O. Rehman, and H. Khan, "Proposal of a new high step-up hybrid switch converter with reduced switch voltage stress," *Int. J. Comput. Sci. Issues (IJCSI)*, vol. 9, no. 5, pp. 263–268, Sep. 2012.
- [47] R. Girish Ganesan and M. Prabhakar, "Multi-level DC-DC converter for high gain applications," *Int. J. Power Electron. Drive Syst.*, vol. 3, no. 4, pp. 365–373, Dec. 2013. doi: <https://doi.org/10.11591/ijpeds.v4i1.4870>.
- [48] A. Ponnirani, K. Orikawa, and J.-I. Itoh, "Modular multi-stage Marx topology for high boost ratio DC/DC converter in HVDC," in *Proc. IEEE Int. Telecommun. Energy Conf. (INTELEC)*, Austin, TX, USA, 2016, pp. 1–6. doi: <https://doi.org/10.1109/INTLEC.2015.7572370>.
- [49] V. Chitransh and M. Veerachary, "A high-gain modular multilevel DC-DC step-up converter," in *Proc. IEEE Int. Conf. Power Electron. Drives Energy Syst. (PEDES)*, Trivandrum, India, 2016, pp. 1–6.
- [50] X. Zhang and T. C. Green, "The modular multilevel converter for high step-up ratio DC-DC conversion," *IEEE Trans. Ind. Electron.*, vol. 62, no. 8, pp. 4925–4936, Aug. 2015. doi: <https://doi.org/10.1109/TIE.2015.2393846>.
- [51] A. Parastar, "High power step-up modular resonant DC/DC converter for offshore wind energy systems," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Pittsburgh, PA, USA, 2014, pp. 3341–3348. doi: <https://doi.org/10.1109/ECCE.2014.6953854>.
- [52] Y. Zhou, L. Jiang, M. Zhang, S. M. Shakh, M. J. B. C. Correa, and W. S. M. A. W. H. Abdullah, "A prototype of modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3267–3278, Jul. 2014. doi: <https://doi.org/10.1109/TPEL.2013.2278338>.
- [53] M. S. Bhaskar, S. Padmanaban, and F. Blaabjerg, "Multistage DC-DC step-up self balanced and magnetic component free converter for photovoltaic applications – Hardware implementation," in *Proc. IEEE Int. Conf. Ind. Technol. (ICIT)*, Toronto, ON, Canada, 2017, pp. 1198–1203.
- [54] R. A. F. I. Mohammad and O. R. A. K. Umar, "A high voltage gain modular multilevel DC/DC converter and inverter fed induction motor," *Int. J. Eng. Res. Technol. (IJERT)*, vol. 4, no. 11, pp. 11159–11168, 2015.
- [55] M. Forouzesh, Y. P. Siwakoti, S. A. Gorji, F. Blaabjerg, and B. Lehman, "Step-up DC-DC converters: A comprehensive review of voltage-boosting techniques, topologies, and applications," *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9143–9178, Dec. 2017. doi: <https://doi.org/10.1109/TPEL.2017.2652318>.
- [56] A. Ponnirani, "A study on optimization of circuit components in high boost ratio DC-DC converters with hybrid-based configuration," Ph.D. dissertation, Dept. Electr. Eng., Nagaoka Univ. Technol., Nagaoka, Japan, 2016.
- [57] A. Ponnirani, K. Orikawa, and J.-I. Itoh, "Fundamental operation of Marx topology for high boost ratio DC-DC converter," *IEEE J. Ind.*

Appl., vol. 5, no. 4, pp. 329–338, Jul. 2016. doi:
<https://doi.org/10.1541/ieejia.5.329>.

- [58] A. Ponniran, K. Orikawa, and J.-I. Itoh, "Interleaved high boost ratio Marx topology DC-DC converter," in *Proc. IEEE 2nd Int. Future Energy Electron. Conf. (IFEEC)*, Taipei, Taiwan, 2015, pp. 1–6. doi:
<https://doi.org/10.1109/IFEEC.2015.7361583>.
- [59] A. M. S. Kumar and S. S. Dash, "Comparison of conventional buck and boost converter with interleaved techniques," *Int. J. Pure Appl. Math.*, vol. 117, no. 16, pp. 205–212, 2017.
- [60] A. Thiyagarajan, "Analysis and comparison of conventional and interleaved DC/DC boost converter," in *Proc. IEEE Int. Conf. Adv. Eng. Technol. (ICAET)*, Nagapattinam, India, 2014, pp. 1–6.